

다중코어의 병렬연산을 위한 컬러링 기법

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KNS Workshop / October 2016

Outlines

- ✓ Introduction : Parallel computation & Coloring method
- ✓ Parallel performance results
 - CPU
 - GPU (based on CUDA)
 - Xeon Phi (Knight landing)
- ✓ Full Multi-Grid (FMG) on the CPU
- ✓ Conclusions

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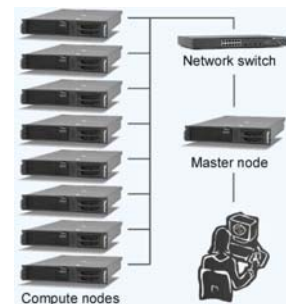
Parallel computation

✓ Classification of devices

- Workstation (MPI, OpenMP)



- Cluster type (MPI, OpenMP)



- GPU (CUDA, OpenCL with MPI)



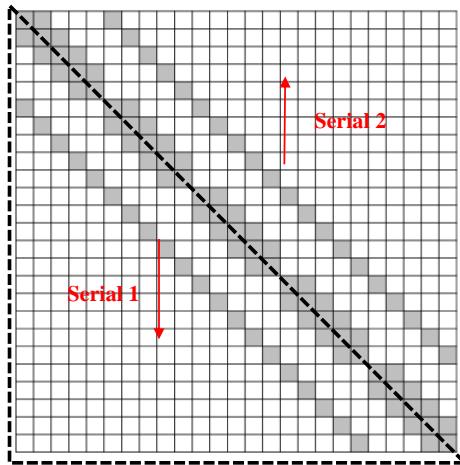
- Xeon Phi (OpenMP, MPI)



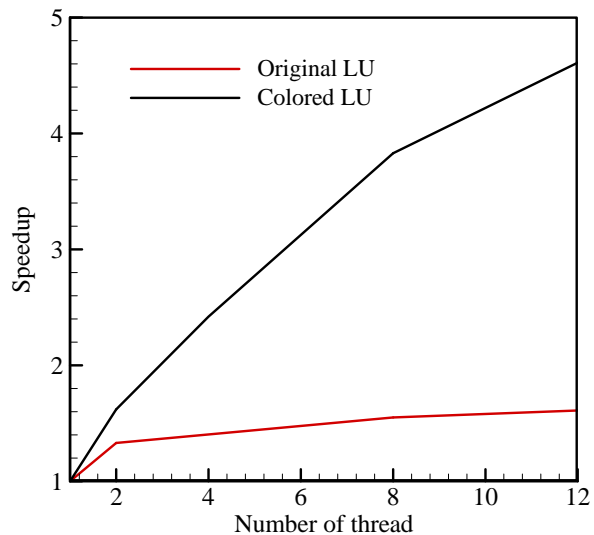
Coloring method for parallel computing

✓ Why use coloring method

	LU / Gauss Siedel Prec.	Jacobi / Digonal Prec.
Characteristics of algorithm	Sequential operation	Independent operation
Convergence	Fast	Slow



LU decomposition operation

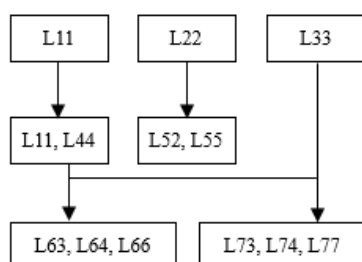
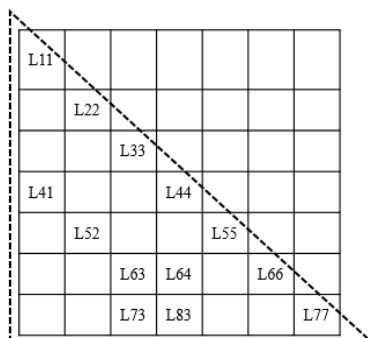


2D Heat conduction problems

Coloring method for parallel computing

✓ What is coloring method

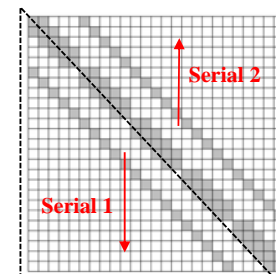
➤ Level Scheduling



➤ Graphic coloring (structured grid)

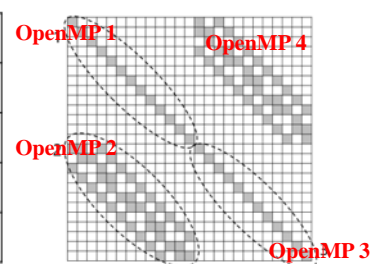
5	10	15	20	25
4	9	14	19	24
3	8	13	18	23
2	7	12	17	22
1	6	11	16	21

Original (Before coloring)



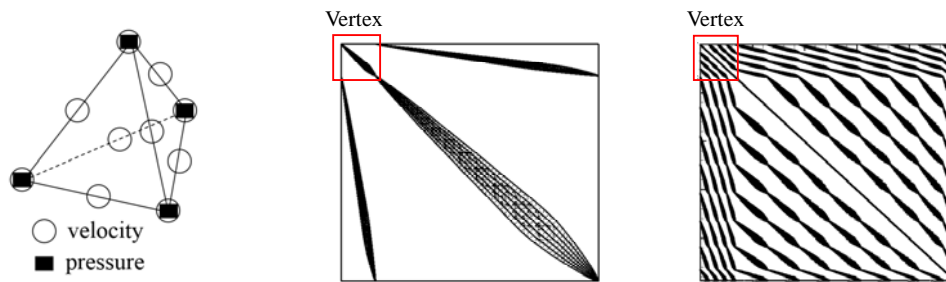
3	18	8	23	13
15	5	20	10	25
2	17	7	22	12
14	4	19	9	24
1	16	6	21	11

After coloring

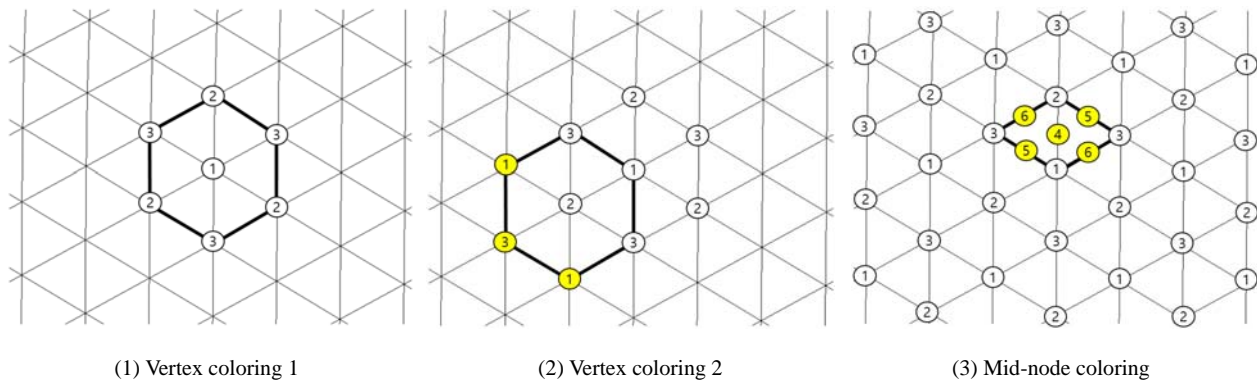


Coloring method for parallel computing

- ✓ Coloring method based on P2P1 element



➤ Coloring process



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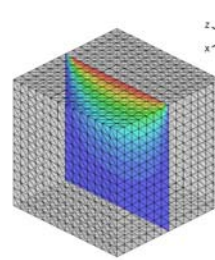
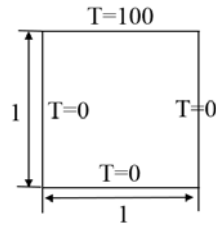
Parallel performance results : CPU

✓ 3D heat conduction problem

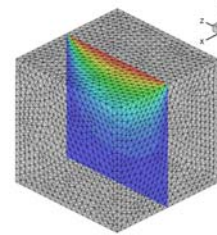
➤ Specification of machine

	Xeon CPU (used 2 CPU)
Model	Intel Xeon CPU E5-2680 v2
Num. core	(10 cores) x2
Clock speed	2.8GHz
Main memory	(16GB x 4slot) x2
Cache Mem	(25MB L3) x2
structure	Rack server
Main board	Supermicro

➤ Schematic and boundary conditions of 3D heat conduction problem

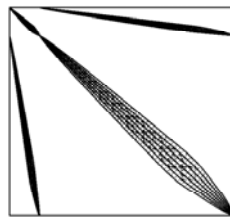


Structured grid

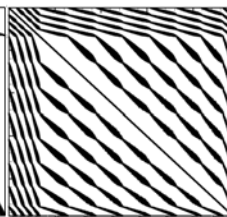


Unstructured grid

➤ Coloring method (FEM)

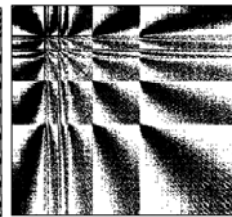


Before coloring

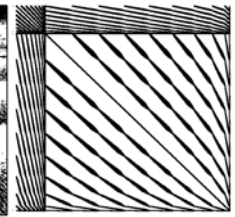


After coloring

Structured grid



Before coloring



After coloring

Unstructured grid

Parallel performance results : CPU

✓ LU preconditioned CG method

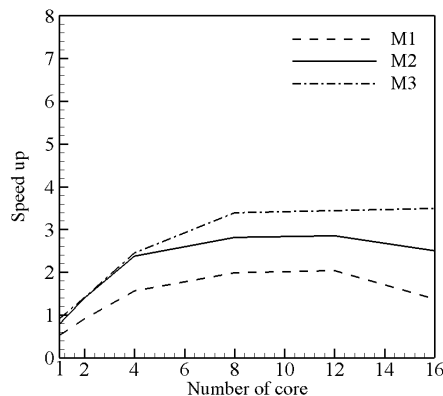
➤ Information of structured grids

Grid	Num. node (P2P1)	Num. color of vertex	Num. color of node (P2P1)
M1	24,389	4	13
M2	68,921	4	13
M3	117,649	4	13

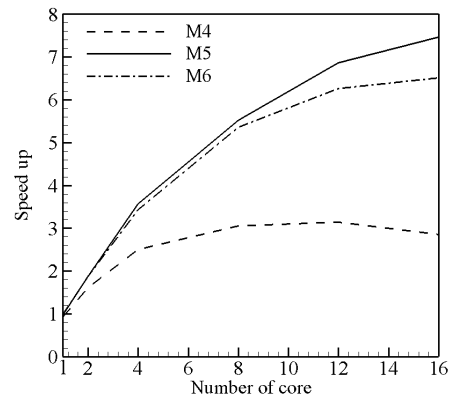
➤ Information of unstructured grids

Grid	Num. node (P2P1)	Num. color of vertex	Num. color of node (P2P1)
M4	25,465	9	19
M5	76,118	9	20
M6	121,796	9	20

➤ Parallel performance of structured grids



➤ Parallel performance of unstructured grids



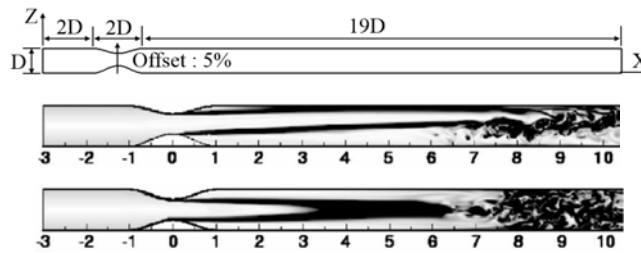
Parallel performance results : CPU

✓ 3D eccentric stenosis problem

➤ Specification of machine

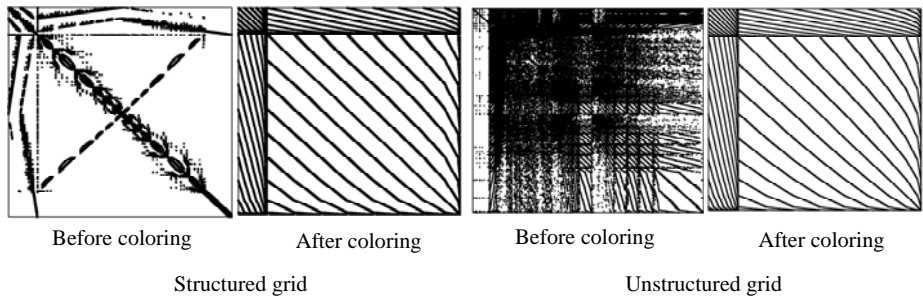
	Xeon CPU (used 2 CPU)
Model	Intel Xeon CPU E5-2680 v2
Num. core	(10 cores) x2
Clock speed	2.8GHz
Main memory	(16GB x 4slot) x2
Cache Mem	(25MB L3) x2
structure	Rack server
Main board	Supermicro

➤ Schematic and boundary conditions



3D eccentric stenosis problem

➤ Coloring method (FEM)



Before coloring

After coloring

Before coloring

After coloring

Structured grid

Unstructured grid

Parallel performance results : CPU

✓ LU preconditioned CG method

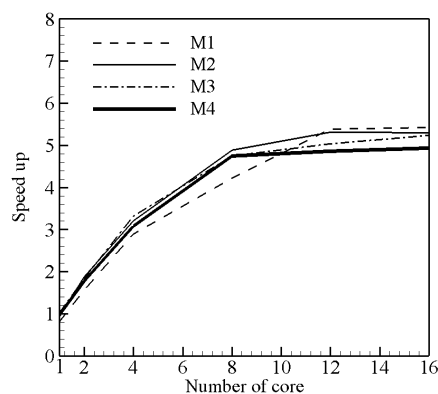
➤ Information of structured grids

Grid	Num. node (P2P1)	Num. color of vertex	Num. color of node (P2P1)
M1	82,761	10	20
M2	158,319	10	21
M3	356,085	9	19
M4	654,497	10	21

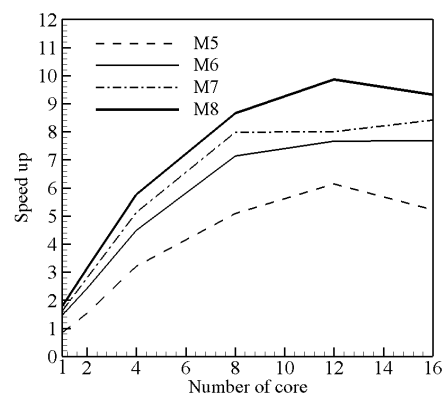
➤ Information of unstructured grids

Grid	Num. node (P2P1)	Num. color of vertex	Num. color of node (P2P1)
M5	80,591	9	19
M6	161,336	9	20
M7	368,826	10	21
M8	674,134	10	21

➤ Parallel performance of structured grids



➤ Parallel performance of unstructured grids

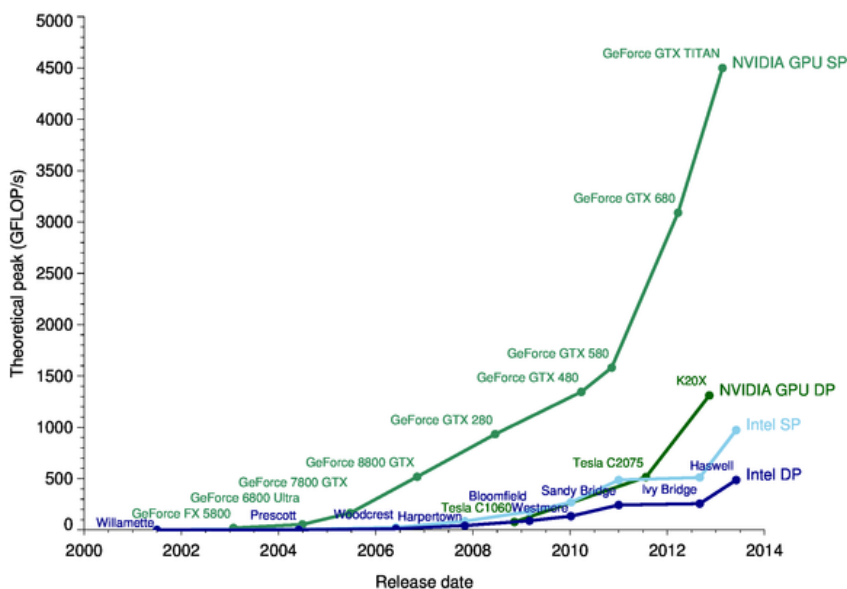


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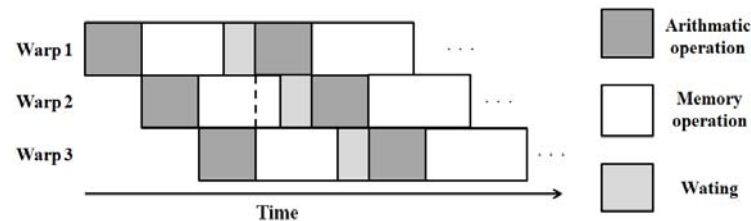
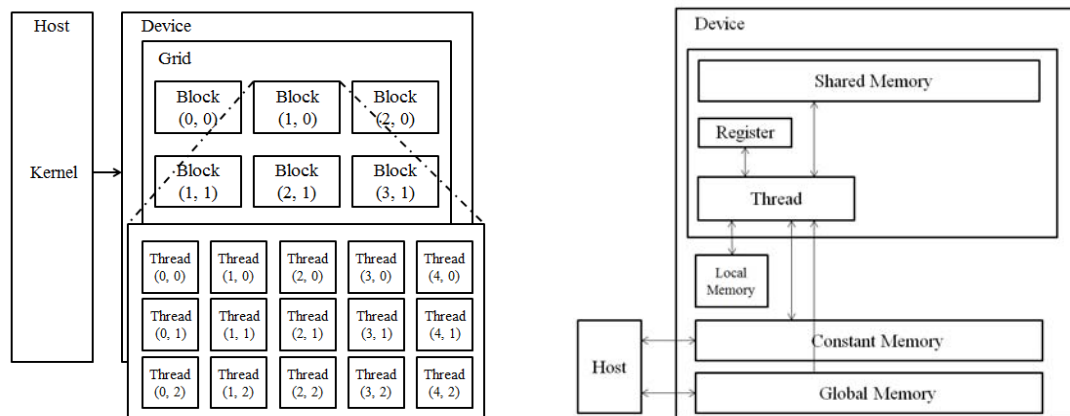
Parallel performance results : GPU

- ✓ Introduction of GPU



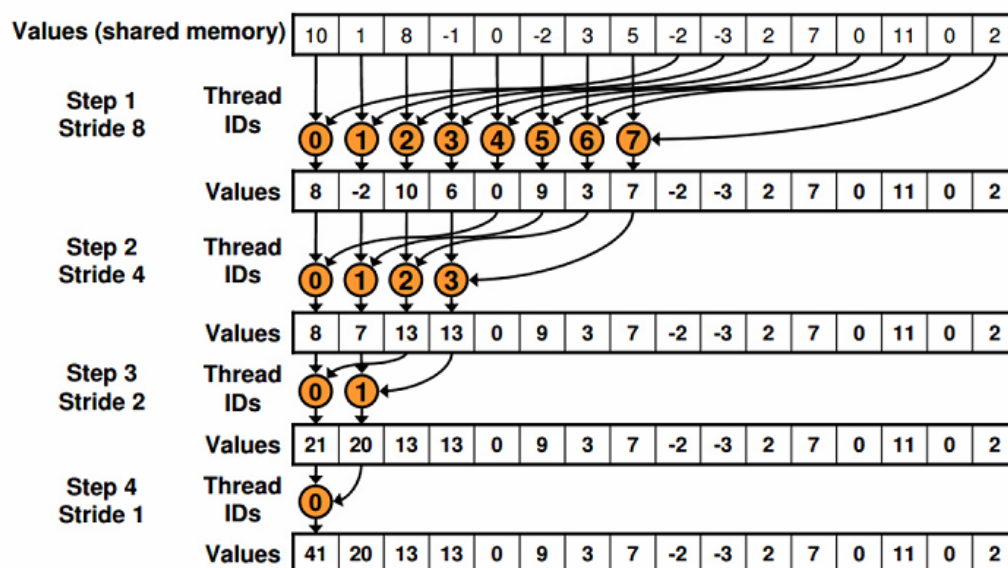
Parallel performance results : GPU

✓ GPU architecture



Parallel performance results : GPU

✓ Reduction with interleaved pairs + unrolling



Number of iteration : 16 → 4

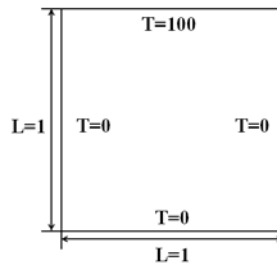
Parallel performance results : GPU

✓ Numerical methods

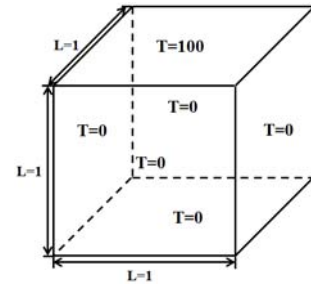
➤ Specification of machine

	Xeon CPU (used 2 CPU)	GPU
Model	Intel Xeon CPU E5-2620 v3	Tesla K40
Num. core	(6 cores) x 2	2880 cores
Clock speed	2.4GHz	745MHz
Main memory	8GB x 4slot	16GB
Cache Mem	(16MB L3) x 2	-
structure	Workstation	Workstation
Main board	Supermicro	Supermicro

➤ Schematic and boundary conditions



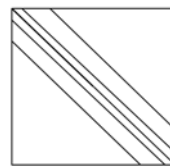
2D heat conduction problem



3D heat conduction problem

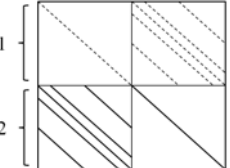
➤ Coloring method (FDM)

13	14	15	16
9	10	11	12
5	6	7	8
1	2	3	4



Before coloring

15	7	16	8
5	13	6	14
11	3	12	4
1	9	2	10

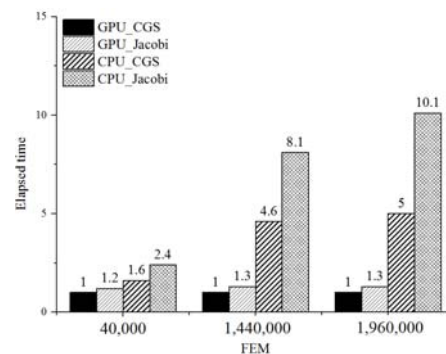
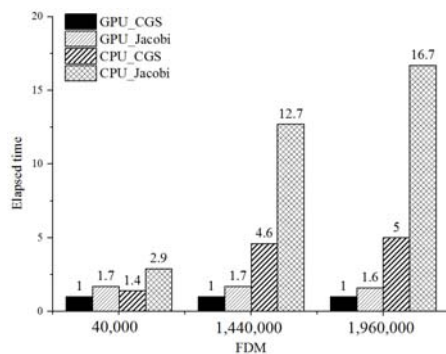


After coloring

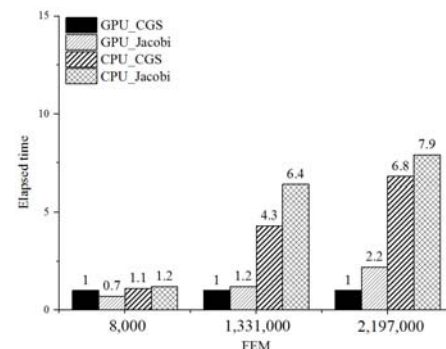
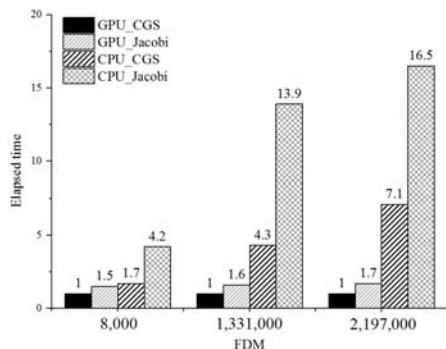
Parallel performance results : GPU

✓ Finite difference method .vs. Finite element method

➤ Elapsed time in 2D problem



➤ Elapsed time in 3D problem



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Xeon Phi (Knight Landing)

- ✓ Introduction of Knight landing (self-boot)



* Intel Xeon Processor Roadmap Plan for HPC

Xeon Phi (Knight Landing)

✓ Advantage of Knights Landing

	Knight Landing	GPU
Code compatibility	Insert OpenMP directive	C++, Fortran → CUDA
Data transfer	On board	PCI Express 3.0
Booting Operating system	Self booting	CPU

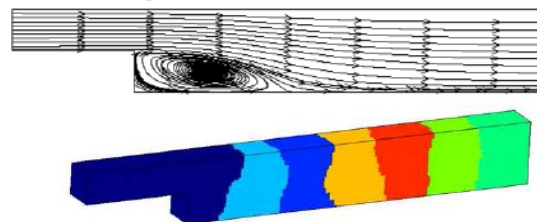
Digonal prec. BiCG solver

✓ 3D backward facing step flow problems

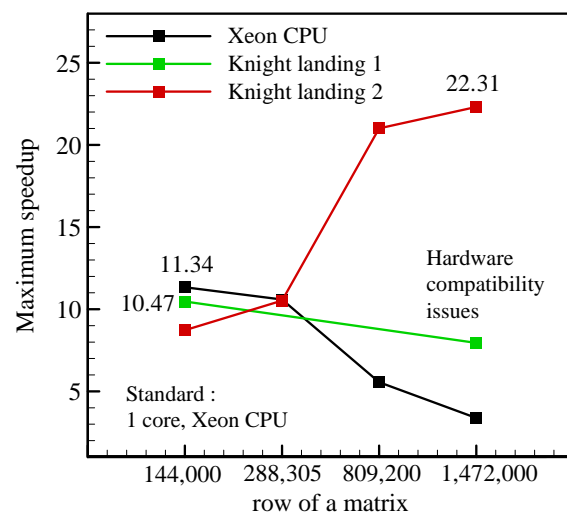
➤ Specification of machine

	Xeon CPU (used 2 CPU)	Knight landing 1	Knight landing 2
Model	Intel Xeon CPU E5-2680 v2	Intel Xeon Phi 7250	Intel Xeon Phi 7210
Num. core	(10 cores) x2	68	64
Clock speed	2.8GHz	1.4GHz	1.3GHz
Main memory	(16GB x 4slot) x2	16GB	16GB
Cache Mem	(25MB L3) x2	34MB L2 (MCDRAM)	32MB L2 (MCDRAM)
structure	Rack server	Rack server	Workstation
Main board	Supermicro	Intel	Supermicro

* Knight landing 테스트는 대한건설링 업체의 지원을 받아 수행되었음.

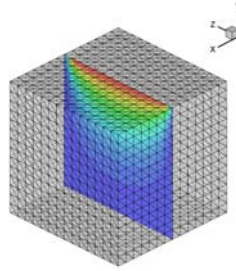


➤ Parallel speedup results

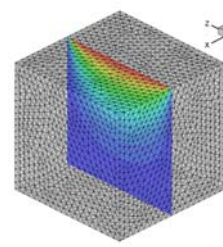
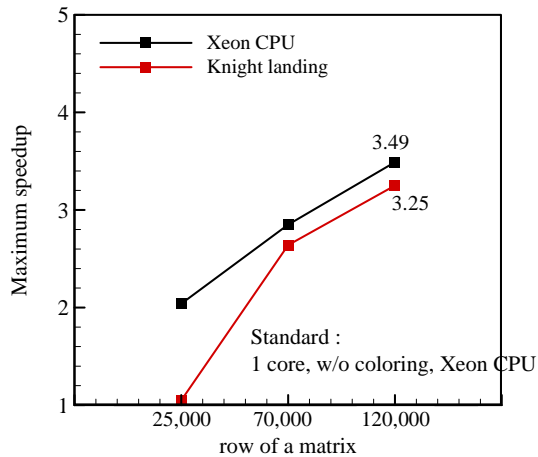


LU prec. BiCG solver with coloring

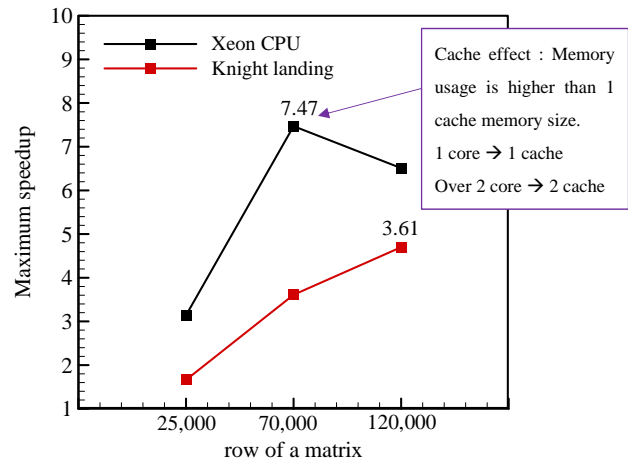
- ✓ 3D heat conduction problems (matrix size : small)



➤ Structured grid

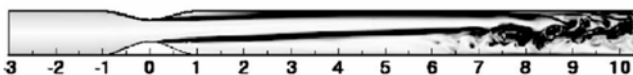


➤ Unstructured grid

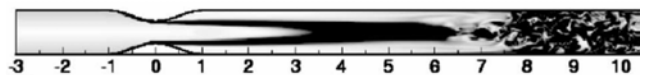
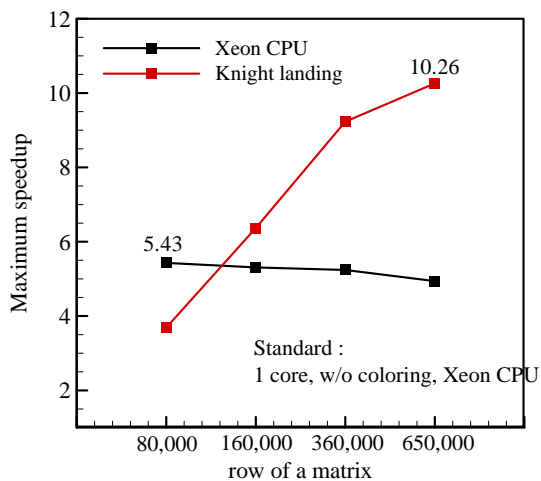


LU prec. BiCG solver with coloring

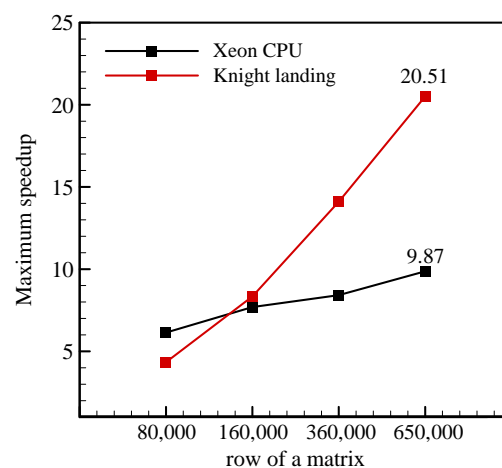
- ✓ 3D heat conduction problems (matrix size : large)



➤ Structured grid



➤ Unstructured grid

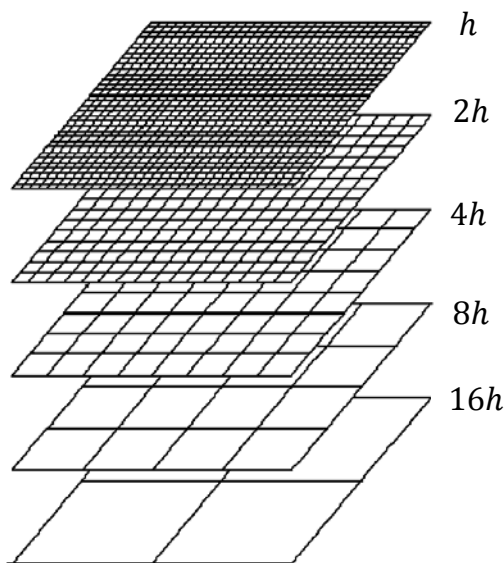


Outlines

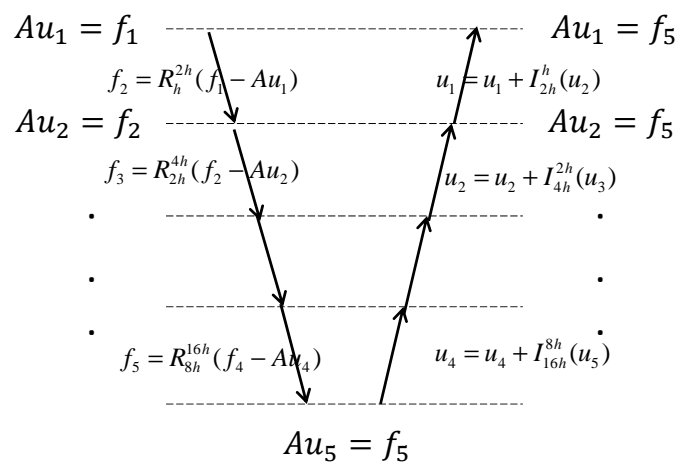
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Full Multi-Grid on the CPU

- ✓ Introduction of Full Multi-Grid for the structured grid



<Multi Level schematic>



<V-cycle schematic>

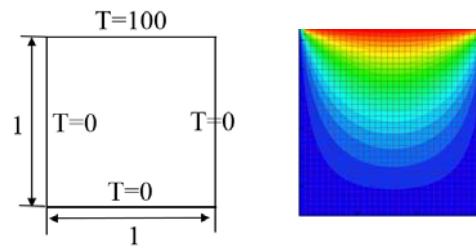
Furture study

✓ 2D heat conduction problem

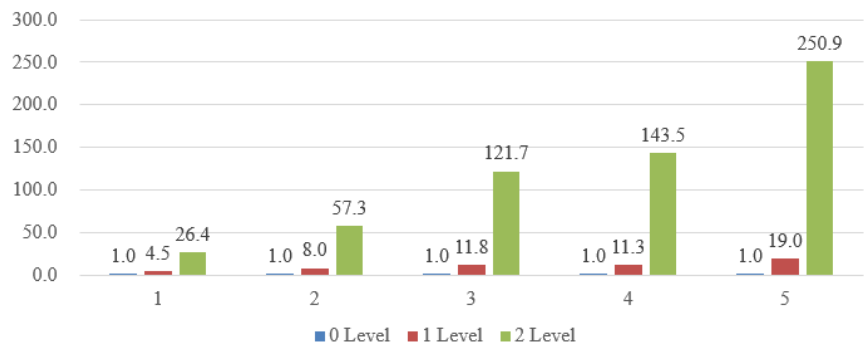
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Main memory	8GB x 4slot
Cache Mem	(16MB L3) x 2
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Main board	Supermicro

➤ Schematic and boundary conditions



➤ Speedup



Thank you!