Development of Testing Platform for Digital I&C System in Nuclear Power Plants

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1. Introduction

According to digitalization of the NPP (Nuclear Power Plant) I&C (Instrumentation & Control) system, cyber threats against I&C system are increased. Moreover, the complexity of I&C system are increased due to adopt the up-to-date technologies (i.e., smart sensor, wireless network, and Field Programmable Gate Array / Complex Programmable Logic Device) into NPP's I&C system. For example, new issues such as cyber threat are introduced from digitalized I&C systems and components to replace obsolete analog equipment in existing NPPs. Furthermore, use of wireless communication, FPGA/CPLD, and smart sensor could introduce new considerations such as Defense-in-Depth and Diversity [1]. Therefore, the proof testing for digital I&C system is required to verify the adverse effect from use of up-to-date digital technologies and identify the criteria to resolve and mitigate (or prevent) the (possibility of) effects. The objective of this study is developing the Testing Platform for the proof testing.

2. Architecture of Digital I&C Testing Platform

The Digital I&C System Test Platform includes platform hardware, software including TSAP (Test Specimen Application Program), and system architecture.

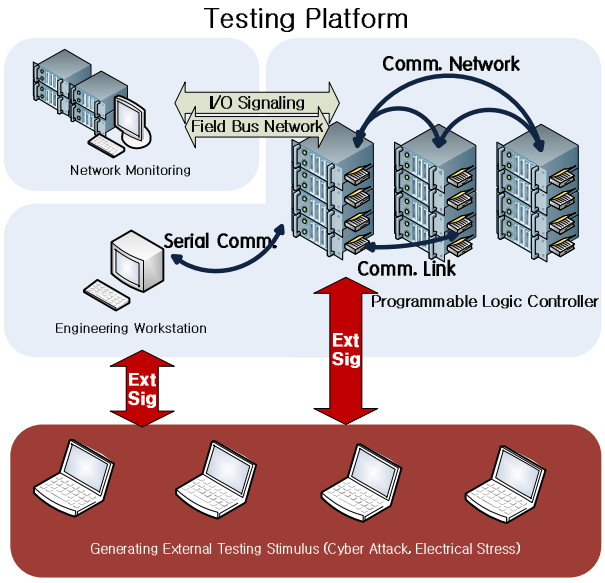


Fig. 1. Overall Digital I&C Testing Platform Architecture

2.1 Hardware Model

Safety-related Programmable Logic Controller (PLC) is selected as a digital I&C system test platform hardware in the consideration of technical support on application programming, etc. Digital I&C system test platform hardware consists of four PLC racks including opto-converting module for interfacing between fiber optic and electrical cable as shown in Figure 1. PCI-E based Network Interface Card (NIC) is installed to interface and monitor communication network of PLCs. Relevant software is developed based on C++ and DotNet of Microsoft. Two USB 2.0 based DAQs (Data AcQuisitions) are installed to interface PLC's analog input/output and digital input/output.

2.2 Software Model

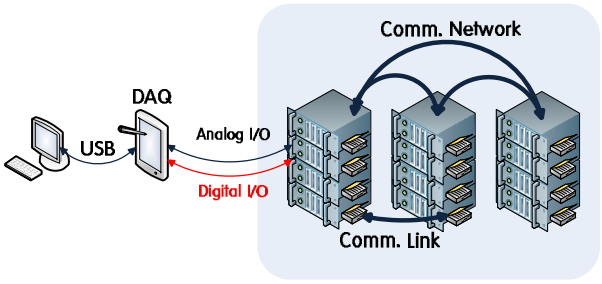
The architectural software of Digital I&C System Test Platform is developed using eXtreme Programming (XP) methodology. The component software for Digital I&C System Test Platform are developed using XP methodology. The objectives of XP programming are for communication between user/customer and designer; Simplicity in design; Feedback from user/customer; and courage on new design [2]. The 12 practices of XP are followings: [2]

- Pair Programming
- Small Release
- Refactoring
- Continuous Integration
- Test Driven Development
- Metaphor
- Planning Game
- Simple Design
- Collective Code Ownership
- 40-Hour Work
- On-site Customer
- Coding Standard

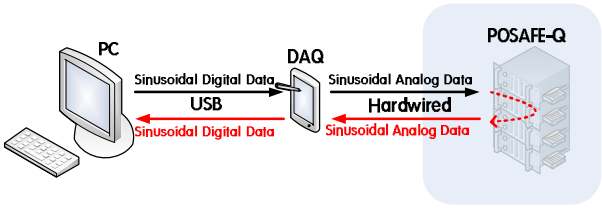
In this study, seven spike models are developed under XP methodology as shown in Table 1. The spike model is a simple code to find the potential solutions against the feasible design bottle-neck or to accommodate the up-to-date technologies into a design. [3] SPIKE_PM is a simple PLC codes to confirm the basic functions of Processor Module and Integrated Design Environment (IDE) for developing the PLC source code. SPIKE_LINK_TX.RX, SPIKE_NET_TX.RX and SPIKE_232_TX.RX are a simple PLC codes to confirm the basic functions of communication modules and to verify its characteristics.

Table 1. List of Spike Model IDs

Spike Model ID	Objectives
SPIKE_PM	- Confirm the functionality of Processor Module and IDE Environment
SPIKE_LINK_TX.RX	- Confirm the functionality of Comm. Link and its characteristics
SPIKE_NET_TX.RX	- Confirm the functionality of Comm. Network and its characteristics
SPIKE_232_TX.RX	- Confirm the functionality of RS-232 Module and its characteristics
SPIKE_AnalogIO	- Confirm the functionality of Analog Input and Output using sinusoidal test signals.
SPIKE_DigitalIO	- Confirm the functionality of Analog Input and Output using sinusoidal test signals
SPIKE_EXTCOMM	- Identify Comm. characteristics such as optical wave-length. - Generate the external interface test signals



(a) Simplified Testing Platform Architecture



(b) Interfacing Connections for I/O Modules

Fig. 2. Overall Digital I&C Testing Platform Architecture

SPIKE_AnalogIO and SPIKE_DigitalIO are a simple PLC codes to confirm the basic functions of various Input/Output modules and to verify its characteristics. SPIKE_EXTCOMM is a Windows-based C++ codes for host PC to generate external stimulus for PLC testing including various communication modules and I/O modules. Since these spike models are module-based code to increase the reusability, these codes are easily integrated into the complicated Test Specimen Application Programs (TSAPs). For example, the test input signals for digital/analog are generated using USB-based DAQ module as shown in Figure 2.

2.3 System Architectural Model

The architecture of digital I&C System Test Platform are selected to represent I&C systems architecture for all NPPs such as RPS (Reactor Protection System), ESF-CCS (Engineered Safety Feature-Component Control System), and RCOPS (Reactor COre Protection System.) The digital I&C System Test Platform is implemented as a form of executable application programs based on the architectural design and relevant component software. However, the executable application programs for test platform will be realized in the next phase.

The digital I&C System Test Platform for acceptance testing against cyber security, smart sensor, wireless network, and FPGA/CPLD is implemented using test platform hardware, component software, and architectural design. Safety-related PLC is selected as a digital I&C System Test Platform hardware in the consideration of technical support on application programming, etc. RPS, ESF-CCS and RCOPS are determined as an architectural design of test platform. The test platform architecture will be design with the objectives of test platform and the consideration of various characteristics such as communication capacity, CPU load, etc. The component software will be developed using XP methodology.

3. Conclusion and Future Work

The digital I&C System Test Platform is implemented using test platform hardware, component software, and architectural design. The digital I&C testing platform includes the safety-related PLC and relevant ladder logics, Windows-based C++ codes for host PC. For software, there are seven spike models to confirm the each module's functionality and generate/monitor the signals to/from PLCs.

For future work, digital I&C System Test Platform architecture will be implemented using spike models. And a set of acceptance test against cyber security, smart sensor, wireless network, and FPGA/CPLD will be conducted using digital I&C System Test Platform.

4. Acknowledgement

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[3] http://www.extremeprogramming.org/