Experience on the FMS Communication module Development for an Application to Safety-Critical Communication Network

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1. Introduction

The field bus has been developed for a network system which supports the real-time communication of various controls and automation equipments. It is known for Profibus in the field of a production automation environment. The Profibus standard uses open communication based on the ISO/OSI model. The Probibus standard uses layer 1, layer 2, layer 7. Layer 7 of Probibus FMS(Fieldbus Message Specification) provides a information and the user of a station.

The high-level communication of the safety-grade PLC (POSAFE-Q) developed through the KNICS(Korea Nuclear I&C System) project is the FMS

This paper describes the design, the configuration, and the test method of the FMS communication module.

2. The Design of NFMS-4Q

The hardware of NFMS-4Q is shown in Figure 1. The CPU that is the XC161CJ manages a communication OS software and The SOC that is the EC-1 manages a communication driver. The CPU is interfacing to a shared memory (CXM), a flash memory, a SRAM. The data exchange between the XC161CJ and the processor module occurs in CXM. EC-1 is a SOC that has the Profibus-FMS protocol and is interfacing to a shared memory (XEM), a flash memory, a SRAM

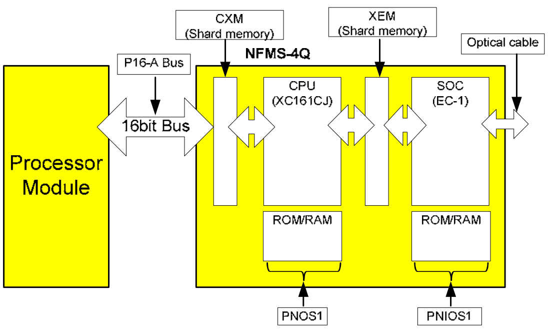

Fig. 1. The configuration of NFMS-4Q hardware

3. The test environment, result and analysis

3.1 The test environment and result

The configuration of NFMS-4Q test environment is shown in Figure 2. The integrity of 30 indexes and the consumption time during the communication are tested. Each FMS scan time is set to 10msec. The master PLC transmits 1~29 index, receives 50~79, 100~129, 150~179 index. The slave PLC receives 0~29 index, transmits 50~79 index. Each dummy receives 0~29 index, transmits 100~129, 150~179 index. The heartbeat is included in transmitting index of master. The heartbeat of each index has the same value and the heartbeat is updated, when the value of 50~79 index received from the slave is same. The updated heartbeat is transmitted to the FMS network. When the value of 0~29 index received from the master is same, the slave transmits 50~79 index to the FMS network.

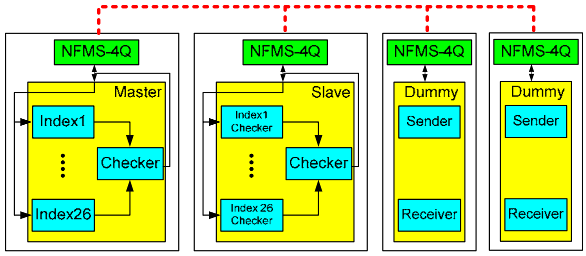

Fig. 2. The configuration of NFMS-4Q test environment

The result of test is as follow

- When a system load is 24%, the response time is 650ms, but most of the response time is 650ms, maximum is 1250ms
- When the system load is 54%, most of the index is transport to the FMS network. But some indexes doesn't transport to the FMS network

3.2 The analysis of the test result

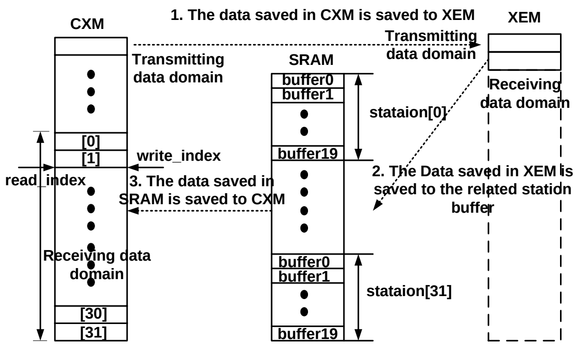

Fig. 3. The process of transmitting and receiving between the shared memories

The mechanism of sending, receiving is described in Figure 3. The process of sending and receiving of NFMS-4Q is as follow

1. If the sending data is exits, the process module saves the data in the transmitting data domain of CXM.
2. After the data saved in CXM is sending to the transmitting domain of XEM, the data is sent to the FMS network.
3. The data received from other station is saved in the receiving data domain of XEM
4. The data saved in XEM is transmitted to the related buffer of station in SRAM.
5. The data saved in SRAM is transmitted to the receiving data domain of CXM
6. The processor module reads the data in CXM

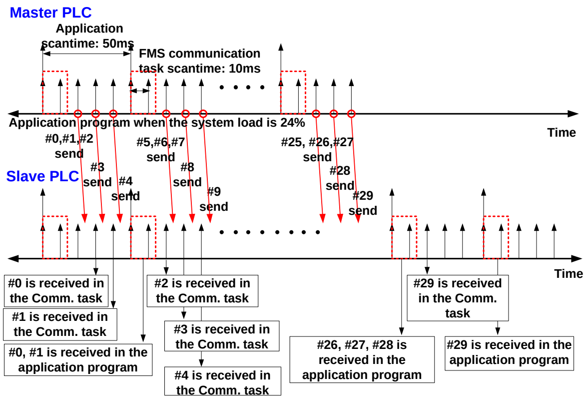

Fig. 4. The sending and receiving process between master and slave in the test environment

In the normal condition, the slave PLC needs 13 scan time to receive all indexes. Then the response time is 650ms if the overflow of SRAM doesn't occur. But FMS Communication task is performed to 3 times of 5 times because of a priority of the FMS communication task. This results in the overflow of SRAM. In the long run, the slave PLC needs 25 scan time (the number of normal scan time: 13 + the number of scan time for the overflow of SRAM: 12) and then the response time is 1250ms.

If the system load is higher, the number of FMS communication task scan time is decreased, because the priority of the FMS communication task is lower than application program. This increases the speed of SRAM overflow and may cause some index not to transport to the FMS network. (Refer to Figure 4)

4. The Modified NFMS-4Q

To resolve the delay of response time and the problem of integrity of data, The NFMS-4Q is modified such as below.

- To improve the delay of response time, The FMS communication task is removed and FMS communication is performed in the application program.
- The configuration of CXM, SRAM is modified and optimized because of the removal of FMS communication task.
- To ensure the integrity of data, the sequence number is checked in application program.

The modified configuration of CXM, SRAM is shown in Figure 5.

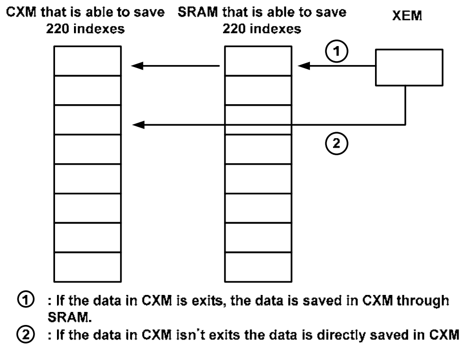

Fig. 5. The modified process sending and receiving between the shard memory

To test the modified NFMS-4Q, the test environment is set to Figure 2. During 3 hours of testing, the response time is 300ms. And the error of CRC, sequence number is not detected. But the periodic data loss occurs because of the difference of master, slave start time in asynchronous system.

5. Conclusions

According to the design criteria of FMS, NFMS-4Q is designed. NFMS-4Q is consisted of the CPU, SOC (EC-1), shared memory (CXM, XEM), SRAM, flash memory. After a testing, the delay of response time and the integrity of data were evaluated because of the priority of FMS communication task, the overflow of the SRAM. So to resolve this problem, the FMS communication task was removed. And CXM, SRAM was modified such as Figure 5. Also, to ensure the integrity of the data, a sequence number check function is added.

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