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A Dead Time Correction for Overlapped Pulse Signals for a Thermal Neutron Coincidence Counter System

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1. Introduction

A typical well-type thermal neutron counter uses many He-3 proportional counter neutron detectors to enhance its measurement efficiency. Such, He-3 detectors are grouped with several other groups to make one output signal. Then the group signals are connected to shift register coincidence electronics using an OR gate device. But a loss of pulse signals occurs in an OR gate device because a simultaneous pulse signal is recognized as one pulse signal. This paper describes the development of a new circuit that processes overlapped pulse signals and the effect of the dead time with an OR gate device of an ACP Safeguards Neutron Counter (ASNC) for an Advanced Spent Fuel Conditioning Process (ACP).

2. Overlapped Pulse Signals and Processing Circuit

A number of He-3 detectors (PDT) are symmetrically located in a high density polyethylene (HDPE) moderator of a thermal neutron counter. The PDT has a two-input logic OR gate input that combines the logic pulses from a self PDT with output pulses from a connected PDT. Combined output pulses pass to the next connected PDT.

The used daisy-chain connection is convenient to use but produces an unnecessary dead-time due to closely following pulses and an overlapping of the pulses. The overlapped pulse signals will be increased more in each group when the grouped output pulses become one pulse stream by using an OR gate device. For this dead-time compensation, the corrected equation for the Singles and Doubles rate are used.

The OR gate dead-time is small compare to the coincidence dead-time. But at high rates, OR gate overlap rate will be increased and observed Singles rate and observed Doubles rate will be decreased. Therefore, if we use a circuit that detects overlapped pulse signals from among grouped pulse signals and processes overlapped pulse signals, the correct value S_m and D_m will be observed.

The processing circuit for the overlapped pulse signals was developed. This circuit has four inputs and one output. At first, the four group pulse signals are checked to see whether they are overlapped. Next, if there are overlapped pulse signals, a pulse generator circuit produces new 50ns pulse width signals. New delayed pulses must have a space of more than 50ns between the pulses. So, a delay line of 120 ns was used. We considered a case where only two pulse signals are overlapped simultaneously. It is reasonable to assume that a triple overlap can not happen simultaneously. Fig. 1 shows the result of a processing when A and B pulse signals are completely overlapped. The pulse signal that corresponds to the B pulse signal is delayed by 120 ns and appears in the output. If the B pulse signal is not processed, the output of the OR gate will only produce one pulse signal. The overlap processing circuit acted well for the 15 ns overlapped pulse, but it did not act as well for the 10 ns overlapped pulse.

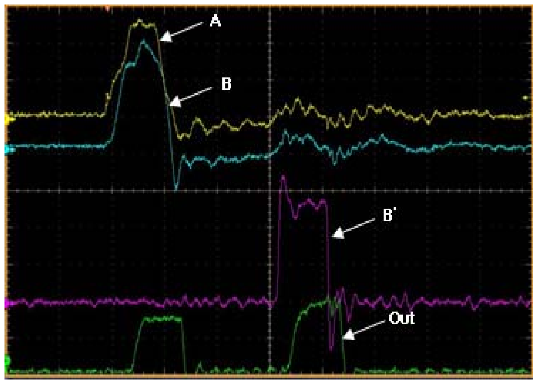

Fig. 1 The A and B pulse signal overlap (50 ns) and output

3. Processing Circuit Test with ACP Safeguards Neutron Counter

KAERI has completed the development of an ACP safeguards neutron counter (ASNC) for a passive non-destructive assay of ACP nuclear materials. We used this ASNC and the overlap test was conducted with a high rate of a ^{252}Cf source which was cross-calibrated at LANL. The neutron intensity of a ^{252}Cf source is 4.053×10^6 n/s on Sept 21, 2005.

Fig. 2 and Fig. 3 show the results of the singles and doubles measurements. Measurement time was 100 s per one cycle and the test cycles were 20 times. “OR Out” is the result of a measurement for the OR gate device (OR box) and “Over Out” is the result where the overlapped pulses are measured and the overlapped pulses are processed. As can be seen in Fig. 2, the singles difference between the OR gate output and Overlap processing circuit is 1.27% (5,883). For the doubles, its difference is much bigger 4.75% (3,094). Its difference is bigger in the doubles because the doubles pulses closely follow more than the singles pulses. The triples are very sensitive to a dead-time. Therefore, the triples difference was very big at 34.7%.

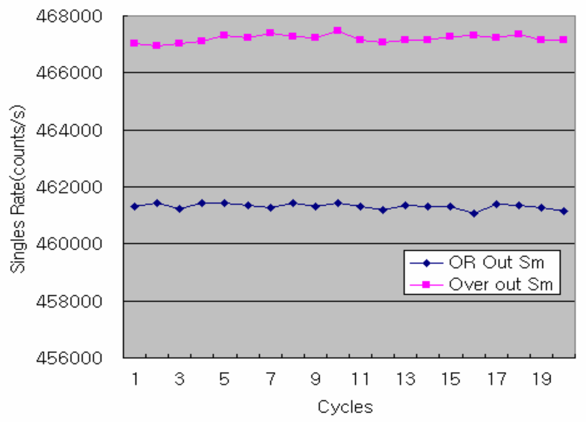

Fig. 2 Result of measurement in singles.

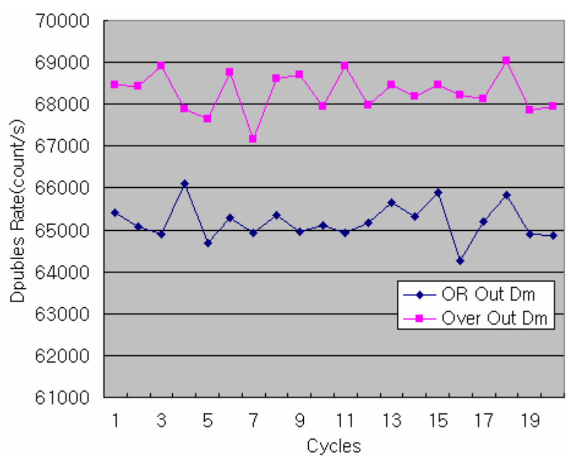

Fig. 3 Result of measurement in doubles

An OR gate overlap rate for the singles is under the assumption that the losses between the channels are due to only a pulse overlap. If applying equation of the OR gate overlap rate for the test at 461k cps, the total losses are calculated to be about 7970 cps and the test result is about 5890 cps. The reason that a difference occurs is explained as follows:

- Process circuit acts when a two pulses overlap is bigger than 10 ns.
- The assumption that no losses occur for a three pulses overlap case.
- Synchronizer dead-time of a shift register. A shift register of a 16 MHz synchronous was used, so the gap that closely follows the pulses must be bigger than 31 ns.

If a three pulses overlap is processed in the added circuit, the loss of a pulse signal will be cleared. Also, the loss of a pulse signal will be solved by the added circuit.

4. Conclusions

We have developed a processing circuit for overlapped pulse signals. The overlapped pulse signals are generated when the pulse signals of a He-3 detector, by using a neutron coincidence counter, are connected to shift register coincidence electronics by an OR gate device. This circuit was tested with an ACP Safeguards Neutron Counter (ASNC) for an Advanced Spent Fuel Conditioning Process (ACP) and a ^{252}Cf neutron source at high rates. In the test of a 461k cps ^{252}Cf neutron source, the loss rate of the output signal was reduced by 1.27% for the singles and 4.75% for the doubles when compared with the OR gate device. Also the variation for the triples was much bigger. Therefore, the pulse signal loss rate can be reduced, if we use an overlap processing circuit instead of an OR gate device. We will develop a processing circuit that closely follows pulse streams for a dead-time reduction in the near future.

Acknowledgement

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