Software of the System Protection for the PEFP 20MeV Proton Linac

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1. Introduction

A 20 MeV proton linear accelerator (linac) has been developed at Proton Engineering Frontier Project (PEFP) [1]. A 20 MeV linac consists of 50 keV proton injector, 3 MeV radio frequency quadrupole (RFQ), and 20 MeV drift tube linac (DTL). PEFP control system is developed with several sub-systems (e.g. machine control, diagnostic control, timing control, and interlock systems). These systems have each EPICS based control system which provides a network-based real time distributed control [2]. For stable and harmonic operation, we had developed sequential logic by using state notation language (SNL) [3] and database records [4] with alarm fields for warning signal. The various control system can drop a transmission rate of the control network traffic. We need to manage control signals by a control network gateway and protect values of control servers by security management. In this paper, the stabilization methods of the control signals are described and the results of the stabilized signals are presented. Figure 1 shows a schematic control system of PEFP 20 MeV proton linear accelerator.

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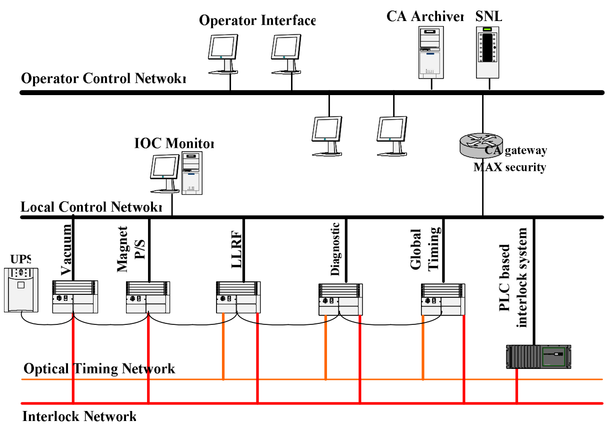

Figure 1 Schematic control system of PEFP 20 MeV proton linear accelerator

2. Stabilization methods on the subsystem

2.1 Vacuum

The devices controlled by EPICS are 2 cryo pumps, 3 gate valves, 2 turbo pumps, and 2 gauges at the RFQ, 8 gauges, 8 turbo-pumps at the DTL. Since all devices of the RFQ are connected to IOC through serial connections, RS422 communication through Signal converter which is relatively safe in wide and noisy environment is used at the RFQ vacuum equipments. The turbo pumps and gauges of the DT were cabled parallel and connected to IOC through Serial/Ethernet Gateway.

We used sequencer of EPICS to implement interlock logics to protect the instruments. The state notation language (SNL) of the sequencer provides a powerful tool for programming sequential operations in a real-time control system like interlock for the control system. The diagram of the simple state transition of the vacuum system for the ion source can see in Figure 2.

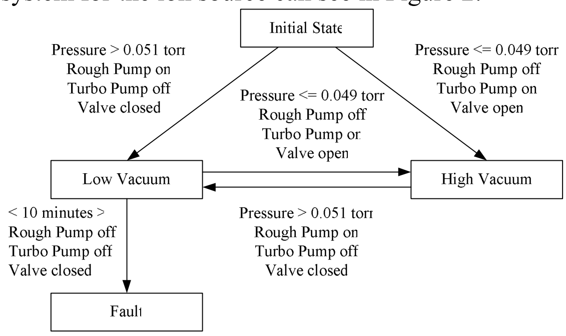

Figure 2 Pressure at initial state classify low and high vacuum. Turbo molecular and scroll pump and gate valve operate routinely at each state. When the pressure stays at low vacuum in some minute sequencer makes a fault state which should be the valve closed, the pump off

2.2 Magnet Power Supply

The IOC server is developed with an async module for analog power supplies and serial I/O driver for digital power supplies. Because the async module supports a low level driver, this can reduce the development cost and time. We have developed an IOC for a power supply of an analog interface operating on the Intel Pentium 4 and Power PC (MVME5100). This system is stably operating. The entire process variables of VME based IOC server have an alarm field. The alarm handler is providing operators with an emergency and warning state. The set value of current and voltage is adjustable through SNL. Alarm signals are applied to software interlock signal.

2.3 Low Level Radio Frequency (LLRF)

The RF amplitude and the phase stability requirements of the accelerating field are within 1% and 1 degree, respectively. As a prototype of the low level radio frequency (LLRF) system, a simple digital proportional integral (PI) control system based on a commercial field programmable gate array (FPGA) board is designed and tested. We have to develop EPICS driver based on interrupt of PMC module. As LLRF protection mode, we have to develop shutdown modules of rf power and rf trigger. EPICS base is the main core of EPICS, comprising the build system and tools, common and OS-interface libraries, Channel Access client and server libraries, static and run-time database access routines, the database processing code, and standard record, device and driver support. Figure 3 shows the schematic structure between LLRF controller and EPICS IOC server program

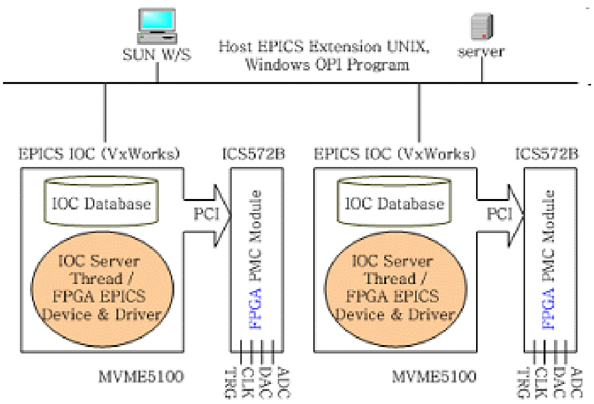

Figure 3 LLRF Control Software Structural Diagram

2.4 Time Synchronization System

The timing system is developed to synchronize the beam pulses of the ion source, the RF systems of the RFQ and DTL, the power supply of the AC switching magnet, and the diagnostic devices. The system is based on an event distribution system, which broadcasts timing information to the sub-components under control.

The timing system should have the following functions:

- Clock synchronization among sub-systems
- RF gate generation
- Beam gate generation
- Triggering for beam diagnostics
- AC magnet gate generation

The protection logic which is implemented in the FPGA of fan-out board is designed to protect the ion source and RF system from beam and RF trigger from the event system by comparing a set pulse width and extracted pulse width as shown in Figure 4.

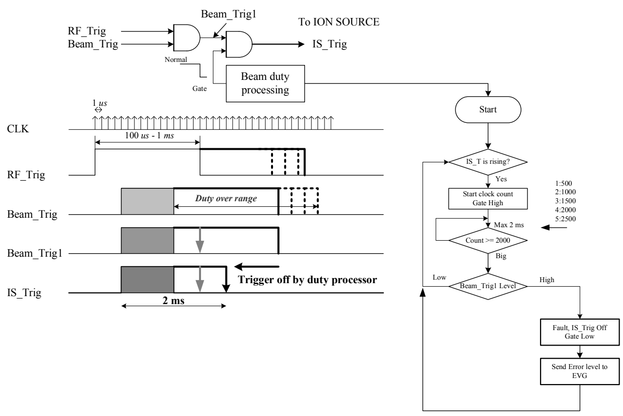

Figure 4 Flow diagrams for the protection of beam trigger pulse

The beam pulses were turned off by an external interlock signal such as a disconnected signal cable or a failure of the power supply system.

3. Control Signal and Access Security Management

We have constructed the gateway to improve a network performance. The Gateway is both a Channel Access Server and Channel Access Client that provides a means for many clients to access a process variable while making only one connection to the server that owns the process variable. We port gateway which supports process variable management.

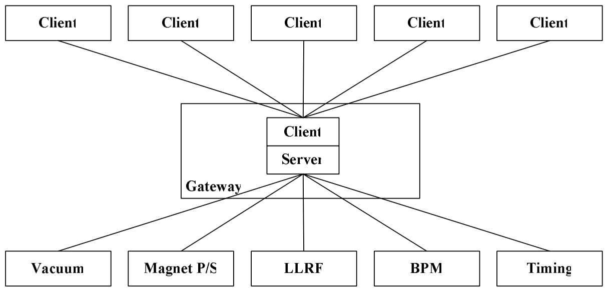

Figure 6 Channel Access viaGateway

All of the IOCs have Access Security which protects IOC database from unauthorized channel access clients. An IOC database can be accessed only via channel access or via the vxWorks shell. It is assumed that access to the local ioc console is protected via physical and telnet access protected via normal Unix and physical security.

4. Summary

After A 20 MeV proton linac is developed at PEFP, we are operating without trouble up to now. Software of the system protection for the PEFP 20 MeV proton linac has been developed as a protection module. The timing system for synchronization of the whole linac system provides a desired pulse signals. The protection logic implemented in FPGA of a fan-out board is responsible for the safe supply of beam and RF trigger. We were able to improve the network transmission rate via Gateway. Also Access security is responsible for a security of the process variables from unauthorized channel clients. We will develop a main protection system into which protection signals can be integrated.

5. Acknowledgements

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Reference

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