Design ASIC by Log Count Rate Circuit for Ex-core Neutron Flux Monitoring System

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1. Introduction

According to the importance about non-memory design is risen recently, interest regarding ASIC(Application Specific Integrated Circuit) design. ASIC is the IC designed and manufactured for specific use. And it also called as Custom IC because, mainly for the semi(-specific) custom LSI, it is designed as the requested specification and drawing by customer. But expense and time loss by failure are becoming big burden to manufacture ASIC actually. Accordingly, provided CPLD(Complex Programmable Logic Device) and FPGA(Field Programmable Gate Array) device with design software can verify before manufacture ASIC.[1] In this paper, Designed and verified LCR(Log Count Rate) circuit for ENFMS(Ex-core Neutron Flux Monitoring System) that is used in plant using ALTERA's CPLD and MAX+PLUS II design tool by Graphic editor with simulation.

2. System Architecture

ENFMS observes neutron continuously so that output of reactor is driven in safety range and operates indication function. ENFMS has safety channels of four, control channels of two and start up channels of two. Totally, eight channels are located near the reactor. Each channel locations are below.

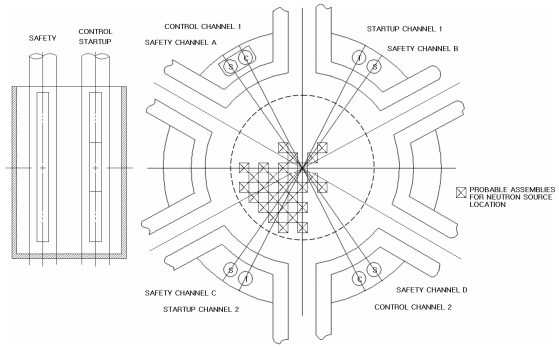

Figure 1. Ex-core Detector locations

Safety channels can measure axis output distribution exactly being consisted of tree sensors which can detect difference range each others. Control channels with built in axial UIC(Uncompensated Ion Chamber) observe output power that is created reactor core upper part and lower part. And start-up channels being consisted of BF_3 comparison calculator operate independently. because parallel calculators are located each channels. One calculator is out of work, the other can help exact function. ENFMS block diagram is below.

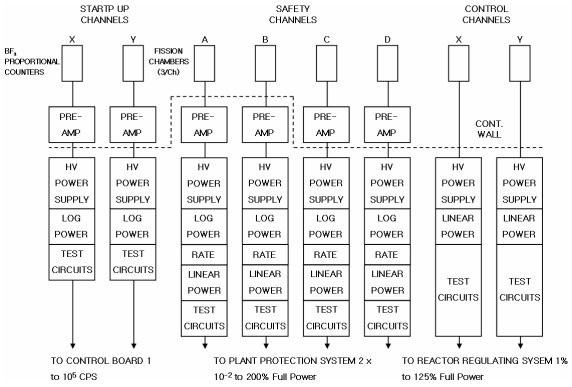

Figure 2. Ex-core Neutron Flux Monitoring System.

Neutron reaction principle to happen in detectors is same with BF_3 comparison calculator like below (1).

$$ {}^{10}_{5}B + {}^{1}_{0}B \rightarrow {}^{7}_{3}Li + {}^{4}_{2}He + 5e^{-} + 2.78MeV \qquad (1) $$

Output signals that come out from detector are small pulse usually, and impedance of detector is very high. So applied pre-amplifier which has high input impedance and send to Discriminator after amplified small pulse to high voltage pulse. Send signal to LCR after separate noise and signal by 'ϒ-layer effect in Discriminator. Change input signal to 0~10[V_{DC}] can use to other systems in LCR.

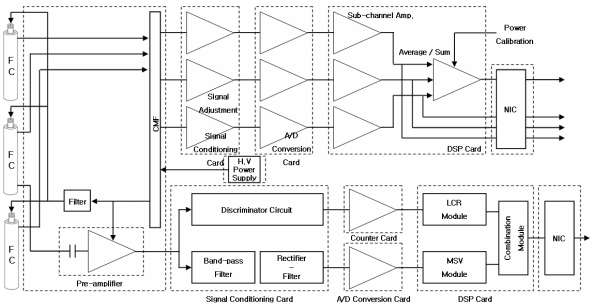

Figure 3. ENFMS Signal processing block diagram

2.1 Circuit and Simulation Result Description

The function of the Log Count Rate(LCR) is to provide an analog output voltage proportional to the log. The output pulses, from the Discriminator/Driver Card to the LCR Card input are approximately 0.1us(TTL Pulse). At high input pulse count rate, the output from the LCR Card is a large positive value. At low input pulse count rate, the output from the LCR Card is biased to Zero. Figure 4 circuit that is consisted of TTL components and simulated in design software.

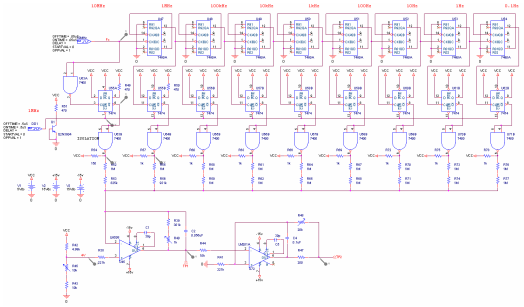

Figure 4. Cadence Pspice designed LCR circuit for simulation.

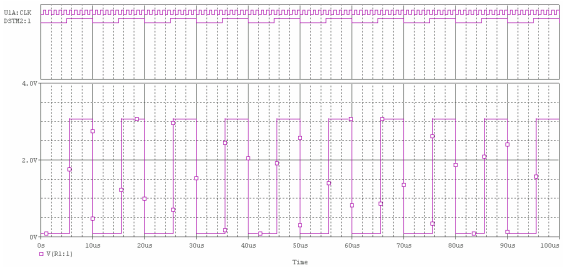

Figure 5. Cadence Pspice simulated result of LCR circuit.

Oscillator A1 produces a 10.0MHz TTL output, which is fed through decade dividers SN7490AN. Refer to figure 00. The clock output and divided outputs in turn are fed in parallel to D flip-flop clock inputs SN7474N. The D inputs of these devices are tied to logical 1, so that as each decade divider in the decade divider chain changes state, it sets its corresponding flip-flop to a logical 1. The inverted output of each flip-flop is fed to NAND Gates, which inverts the sense of the input and provides isolation between the flip-flops and filter networks.[2]

Each flip-flop therefore receives the same reset pulse frequency(f_r), but differing clock frequencies(f_c) dependent on which decade divider provides its input. The average output of each tank circuit is dependent on the ratio of f_r to f_c, being greatest when f_r is much less than f_c, at which time the output approaches +5Vdc. With very low count rate inputs, f_r will be much lower than f_c in most tank circuits, therefore, maximum output will be derived from the NAND Gates, and the output of 1st OP-Amp would be a large negative value, since it is operating in the inverting mode.

The output of 1st OP-Amp is biased to zero at very low count rates using input resistor. At high count rates, there is very little output from most tank circuits, so that the output of 1st OP-Amp becomes a large positive value which follows the NAND Gates. The resistors in series with each NAND Gate output serve as input resistors to summing operational amplifier 1st OP-Amp. The capacitors which are placed near the resistor filter the AC ripple on the NAND Gate outputs. Each gate will exhibit an average output voltage that is related to the input count rate.

2nd OP-Amp and Feed-Back resistor provide scaling adjustment so that a slope of two volts of output for each decade increase in input can be achieved.

Following Figure 6 and 7 are designed LCR circuit partially and simulated for programming at CPLD. As simulation result, it can get almost same output result.

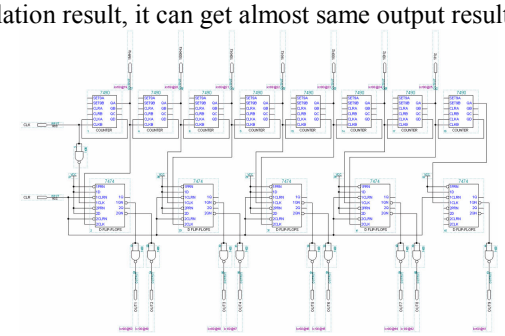

Figure 6. ALTERA MAX+PLUS II designed LCR circuit by graphic editor.

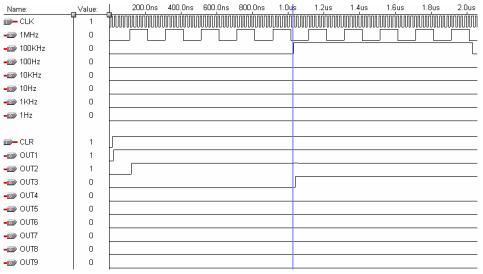

Figure 7. ALTERA MAX+PLUS II simulated result of LCR circuit.

Finally, Compared result with existing circuit which consist of TTL component and circuit which consist of CPLD after programming by output signal. Excepted noise that is included to output, it can get similar output.

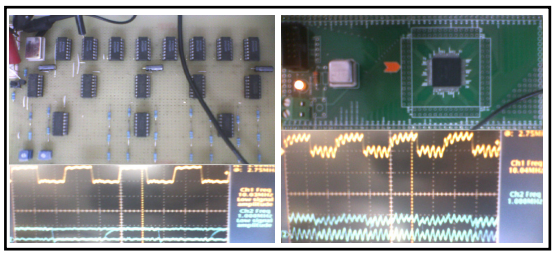

Figure 8. LCR Circuit which consist of TTL component (a) and consist of CPLD (b).

3. Conclusion

The purpose of this paper is to introduce a method of design ASIC that is used to CPLD for specific circuit. the existed LCR circuit by almost TTL component replaced a circuit by designed LCR circuit to ASIC, it made increased reliability, decreased power consumption. Beside, there is an advantage that can keep design technology in CPLD. It can also design Full-Custom IC if no more change circuit From now on.

REFERENCES

[1] Lee seung ho, “Design Digital Logic Circuit using ALTERA MAX+PLUS II”, p.2, 2003.

[2] Norman Balabanian, Bradley Carlson, “Digital Logic Design Principles”, Wiley, 2001.