FPGA Design Methodologies Applicable to Nuclear Power Plants

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1. Introduction

Analog-based equipment in I&C(Instrumentation & Control) systems of operating NPPs(Nuclear Power Plants) has been replaced with microprocessor-based digital equipment as it becomes obsolete. And I&C systems of new NPPs also have been designed to adopt the digital equipment such as PLC(Programmable Logic Controller) and DCS(Distributed Control System). But software like operating system and application program in the digital equipment may not be simply qualified because of its complex characteristics[1].

In order to solve the above problem, NPPs in some countries such as the US, Canada and Japan have already applied FPGA-based equipment which has advantages as follows[1]: 1) It is easier to verify the performance because it needs only HDL code to configure logic circuits without other software, compared to microprocessor-based equipment, 2) It is much cheaper than ASIC in a small quantity, 3) Its logic circuits are reconfigurable, 4) It has enough resources like logic blocks and memory blocks to implement I&C functions, 5) Multiple functions can be implemented in a FPGA chip, 6) It is stronger with respect to cyber security than microprocessor-based equipment because its configuration cannot be changed by external access, 7) It is simple to replace it with new one when it is obsolete, 8) Its power consumption is lower.

However, FPGA-based equipment does not have only the merits. There are some issues on its application to NPPs. First of all, the experiences in applying it to NPPs are much less than to other industries, and international standards or guidelines are also very few. And there is the small number of FPGA platforms for I&C systems. Finally, the specific guidelines on FPGA design are required because the design has both hardware and software characteristics [5].

In order to handle the above issues, KINS(Korea Institute of Nuclear Safety) built a test platform last year and have developed regulatory guidelines for FPGA-application in NPPs[6].

2. FPGA Architecture and Design Flow

FPGA consists of CLB(Configurable Logic Block), I/O block, memory, internal interconnection grid and other components in general. Figure 1 shows the FPGA architecture[1].

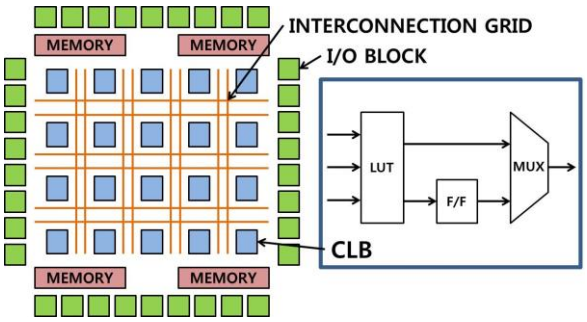

Figure 1. FPGA Architecture

CLB is used to configure logic circuits for I&C functions and consists of LUT(Look Up Table), flip-flop and multiplexer. And multiple CLBs are connected with each other by using internal interconnection grid to configure the larger logics. Voltage, current and direction(input, output, bi-direction) of digital signals through FPGA pins are set up in I/O blocks. Memory is used to write and read data which are necessary to implement I&C functions.

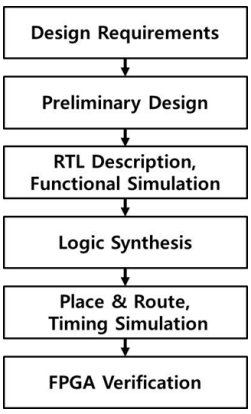

Figure 2. FPGA Design Flow

A general flow of FPGA design is as Figure 2. The requirements for functionality and performance of the final FPGA chip are usually defined in the first step of the design flow. In the next step, the designers should determine the hierarchical structure of modules for configuring the logic circuits and select pre-developed items such as IP(Intellectual Property) and library which are used in FPGA design. In RTL(Register Transfer Level) description step, the logic circuits including IPs and libraries are expressed by HDL(Hardware Description Language). HDLs commonly used in the design are VHDL and Verilog HDL. The RTL description is circuit-independent and can be easily

applied to other FPGA chips. And the logic circuits expressed by HDL are verified in functional simulation. Each component of the RTL logics is mapped into a real resource of the designed FPGA through logic synthesis. During P&R(Place and Route) process, the mapped resources are placed and routed to meet the timing constraints specified by FPGA designers. The objective of the constraints is to ensure that no timing violations (period, setup or hold violation) will occur when FPGA circuits are normally working. In the last step, the functionality and performance of the designed FPGA are verified through checking if the final logic circuits operate as the simulation results by measuring pins or internal states.

3. FPGA Design Guidelines

Software tools may be able to optimally implement the logic circuits to meet the specified constraints during the synthesis and P&R process. But the best way of FPGA design is appropriately describing the RTL expressions considering the logic circuits to be physically implemented.

This paper describes the essential design guidelines applicable to FPGA-based equipment in I&C systems after reviewing the related technical reports and general FPGA design rules[1][2][3][4].

- Static timing analysis for asynchronous logics cannot be conducted. Therefore, synchronous logics should be implemented to avoid glitch, skew and other timing violations. If asynchronous logics are used for specific purpose, they should be split up with the synchronous logics, and their timing information such as signal delays should be provided by the designers.
- Enough time to determine an output state of flip-flop should be considered when asynchronous signals are connected to synchronous logic blocks. Figure 3 shows an example of metastability. Q_A may not be determined because of the unstable input at the rising edge of the clock. This result also causes an error of Q_B because Q_A is unstable at the falling edge of the clock.

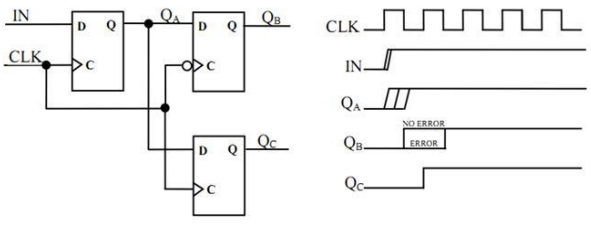

Figure 3. An Example of Metastability

- Timing constraints including period, skew and propagation delay between internal components are very important to implement logic circuits having enough timing margins during P&R process. The designers should select values of the constraints carefully because the values can directly affect the performance of the logics.
- After the logic synthesis, unintended latch should not be created especially in the design of safe-related functions. That is because edge-triggered flip-flop is much better than level-sensitive in the sequential and synchronous logic circuits. If the latch is necessary to be implemented, it should be expressed explicitly by RTL description.
- Gated clock should not be used in the logic circuits because it may cause clock skew. The skew affects clock timing adversely and results in performance degradation such as glitch and race. Therefore, the output of flip-flop should not be connected to a clock pin of another flip-flop.
- Each output corresponding to each of the all input combinations should be defined explicitly in the logics of state machine and multiplexer. In other word, default state should be described even for unused input combinations. That is because unintended latch may be created or undefined state may be selected by noise occurred in input signals.

4. Conclusions

I&C systems of NPPs have been increasingly using FPGA-based equipment as an alternative of microprocessor-based equipment which is not simple to be evaluated for safety due to its complexity. This paper explained the FPGA design flow and design guidelines. Those methodologies can be used as the guidelines on FPGA verification for safety of I&C systems.

5. Acknowledgement

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REFERENCES

[1] EPRI 1019181, “Guidelines on the Use of Field Programmable Gate Arrays (FPGAs) in Nuclear Power Plant I&C Systems”, 2009.
[2] NUREG/CR-7006, “Review Guidelines for Field-Programmable Gate Arrays in Nuclear Power Plant Safety Systems”, 2010.
[3] IEC 62566, “Nuclear Power Plants–Instrumentation and control important to safety–Development of HDL-programmed integrated circuits for systems performing category A functions”, 2012.
[4] Ciletti, Michael D., “Advanced Digital Design with the Verilog HDL”, Prentice-Hall, 2010.
[5] G.Y. Park, Y.G. Yoo, H. T. Kim, Y.I. Kwon and C. H. Jeong, Regulatory Issues on Using Programmable Logic Device in Nuclear Power Plants, KNS Autumn Meeting, 2012.
[6] Young-Mi Kim and Yong-Il Kwon, Development of Test Platform for Digital I&C System Evaluation, KNS Autumn Meeting, 2012.