FPGA Design and Verification Procedure for Nuclear Power Plant MMIS

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Abstract

Currently, the PLC (Programmable Logic Controller) which is being developed is composed of the FPGA (Field Programmable Gate Array) and CPU (Central Processing Unit).

As the importance of the FPGA in the NPP (Nuclear Power Plant) MMIS (Man-Machine Interface System) has been increasing than before, the research on the verification of the FPGA has being more and more concentrated recently.

In this paper, it is shown that it is possible to ensure reliability by performing the steps of the verification based on the FPGA development methodology, to ensure the safety of application to the NPP MMIS of the FPGA run along the step.

1. Introduction

Based on the V-model, verification methods from the existing NPP PLC was carried out for Software-based verification. (Shown in Figure 1) Implementation of these processes has a lot of problems in the methodology of the development and validation of the FPGA based the Hardware. To solve these problems, by applying the design techniques SoC (System on a Chip) commercial provides a method of increasing the flexibility and reliability of the verification of development. (Shown in Figure 2)

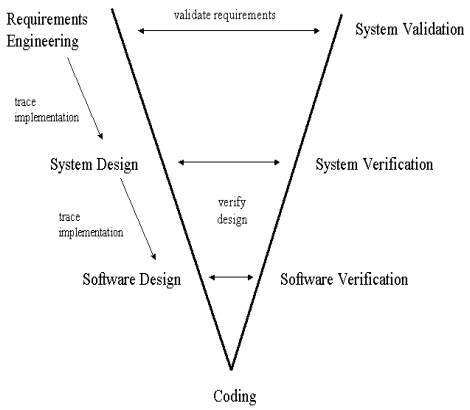

Figure 1 the V-modle of the systems engineering process

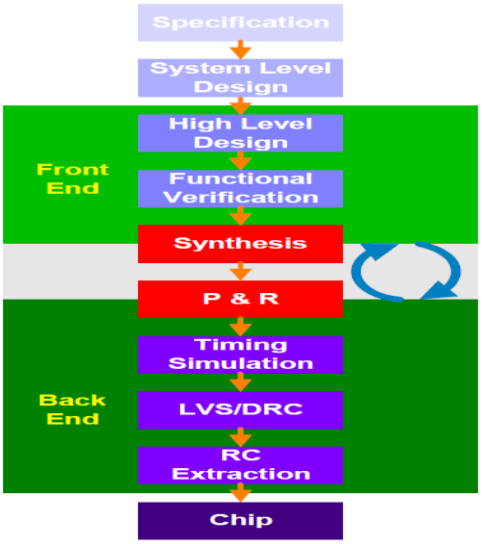

Figure 2 the design techniques SoC

2. Proposed Verification and Developments Methods

The design IP (Intellectual Property) is how to develop SoC general, when you run the V&V (Verification and Validation) for the IP of each, how to develop and validate the proposed increase the reliability of the features of IP. It is a method to perform the function of a FPGA making the Top-module which is combination of thus made the IPs. Hardware verification was carried out at the existing Board Level. In other words the FPGA environment, the peripheral device is not allowed access to the internal core of the physical FPGA during testing of the system, verification of Board Level Hardware, the observation of each peripheral device was possible. In order to solve it, it is necessary to separate out verification IP.

To perform this method, it is necessary to analyze the exact system requirements, the division of each Component specific features you must clear. Verification of IP, which is divided each function, is performed timing, implementation and test. We propose three times validating Top-module what is a combination of the validated IPs. (Shown in Figure 3)

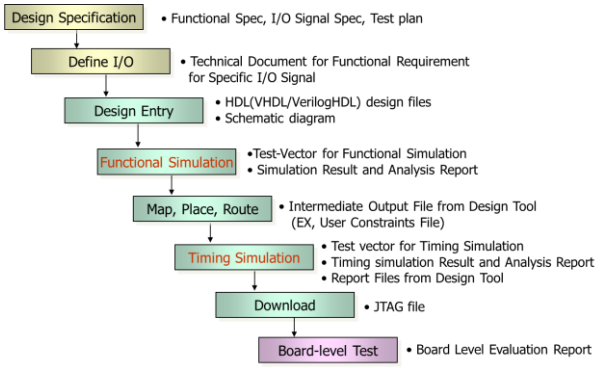

Figure 3 the verification and developments methods

2.1 Design Specification

We analyze design specifications, defined specifications, the specifications for each I/O (Input/Output) functions, respectively. This is the first work to design separate the IPs. I also determined in advance the Test Case for each IP.

2.2 Define I/O

FPGA pin shall be placed in accordance with the performance and functionality of the peripheral Hardware. Prior to the circuit design, I consider so as not affecting the timing and signal.

2.3 Design Entry

Block Diagram to design according to the design specifications. The designing shall use HDL (Hardware Description Language, such as VHDL or Verilog) according to the features and the Pin-assign of Block Diagram.

2.4 Functional Simulation

Logic is formed in the RTL (Register transfer level) what is the designed HDL. Each IP will be performed to the functional simulation. The functional simulation is only simple functions simulation except the timing delay. Also, it shall run functional simulation about the Top-module after finishing the functional simulation.

2.5 Map, Place, Route

If the Functional Simulation complete successfully, the designed RTL will placed in a cell inside the FPGA.

2.6 Timing Simulation

It did not apply in the Timing Delay Function Simulation, file is generated SDF (Standard Delay Format) after the P&R (Place and Route), which contains information Delay. You can then use it to the Simulation of Delay inside the actual FPGA.

2.7 Download

To be able to operate as a chip download through the JTAG (Joint Test Action Group) from files that has knowledge of P&R of Logic Cell of the FPGA.

2.8 Board-level Test

After the download to FPGA final design has been completed and tested using the Logic Analyzer a signal at Board level. (Shown in Figure 4)

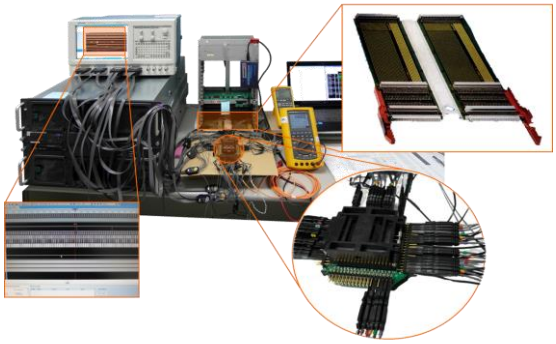

Figure 4 tested using the logic analyzer

3. Conclusions

In developing the FPGA in the V model, which was provided for software development, has seen a number of limitations on the development of hardware-based FPGA. By To solve these problems, the design and verification by applying the design method IP used in the SoC general, has been verified to see a visual software items designed to HDL, the P&R after you go through the process and verification of hardware and software to the intermediate time.

Finally, after the actual downloaded to the FPGA, in hardware verification Board level. In this way, then it is possible to complement the V model that was developed showing the limits on the FPGA, in fact, I propose a method can be designed to suit the FPGA.

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