FPGA Design and Verification Procedure for Nuclear Power Plant MMIS

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CONTENTS

- Introduction
- Software Life-Cycle
- General PLD Design & Verification method
- PLD development using V-model
- Life-Cycle of Codes & Standards
- Proposed Verification and Development Method
- Recommend Life-Cycle
- Conclusion

Introduction

- Based on the V-model, verification methods from the existing NPP PLC was carried out for Software-based verification.

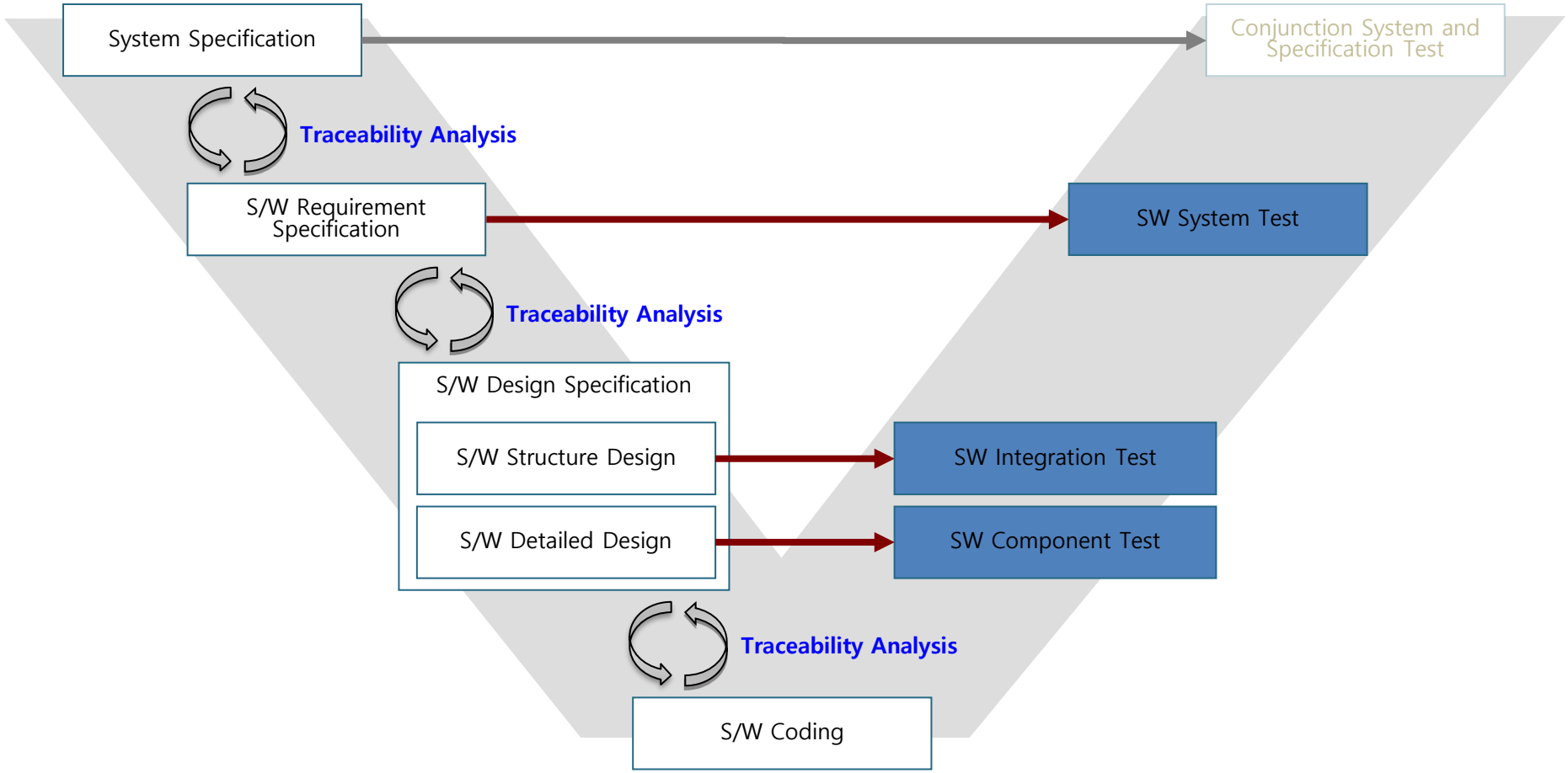
- Implementation of these processes has a lot of problems in the methodology of the development and validation of the FPGA based the Hardware.

- To solve these problems, by applying the design techniques SoC (System on a Chip) commercial provides a method of increasing the flexibility and reliability of the verification of development.

Software Life Cycle

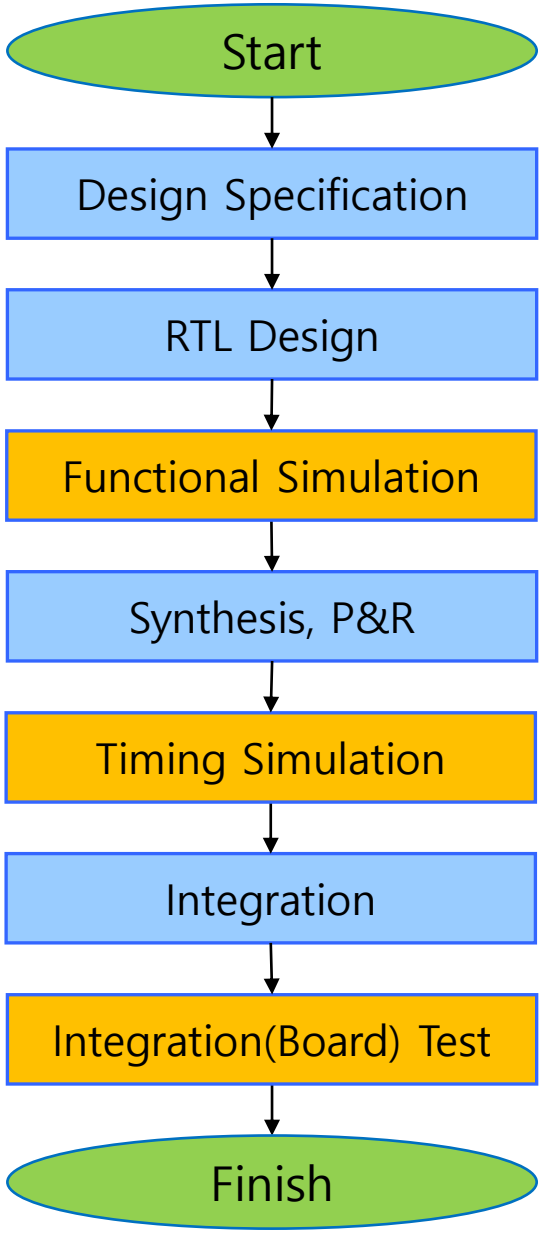
Plan Phase

IEEE1074 Software Life Cycle (V-Model)



→ V-Cycle Verification & Validation

General PLD Design method



Design Specification

: We analyze design specifications, defined specifications, the specifications for each I/O functions, respectively. This is the first work to design separate the IPs. I also determined in advance the Test Case for each IP.

RTL Design

: The designing shall use HDL (Hardware Description Language, such as VHDL or Verilog) according to the features and the Pin-assign of Block Diagram.

Synthesis, Place & Route

: If the Functional Simulation complete successfully, the designed RTL will placed in a cell inside the FPGA.

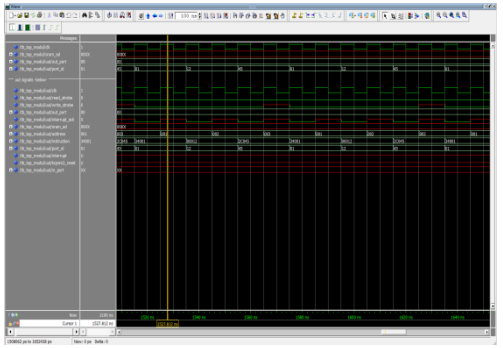
Integration

: To be able to operate as a chip download through the JTAG (Joint Test Action Group) from files that has knowledge of P&R of Logic Cell of the FPGA..

General PLD Verification method

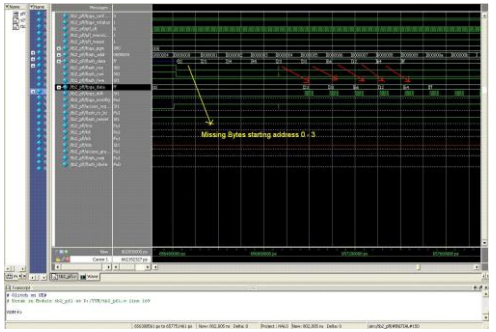
Functional Simulation

: Logic is formed in the RTL what is the designed HDL. Each IP will be performed to the functional simulation. The functional simulation is only simple functions simulation except the timing delay. Also, it shall run functional simulation about the Top-module after finishing the functional simulation.



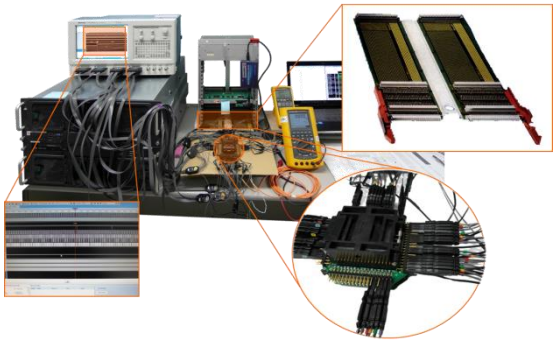
Timing Simulation

: It did not apply in the Timing Delay Function Simulation, file is generated SDF (Standard Delay Format) after the P&R (Place and Route), which contains information Delay. You can then use it to the Simulation of Delay inside the actual FPGA.



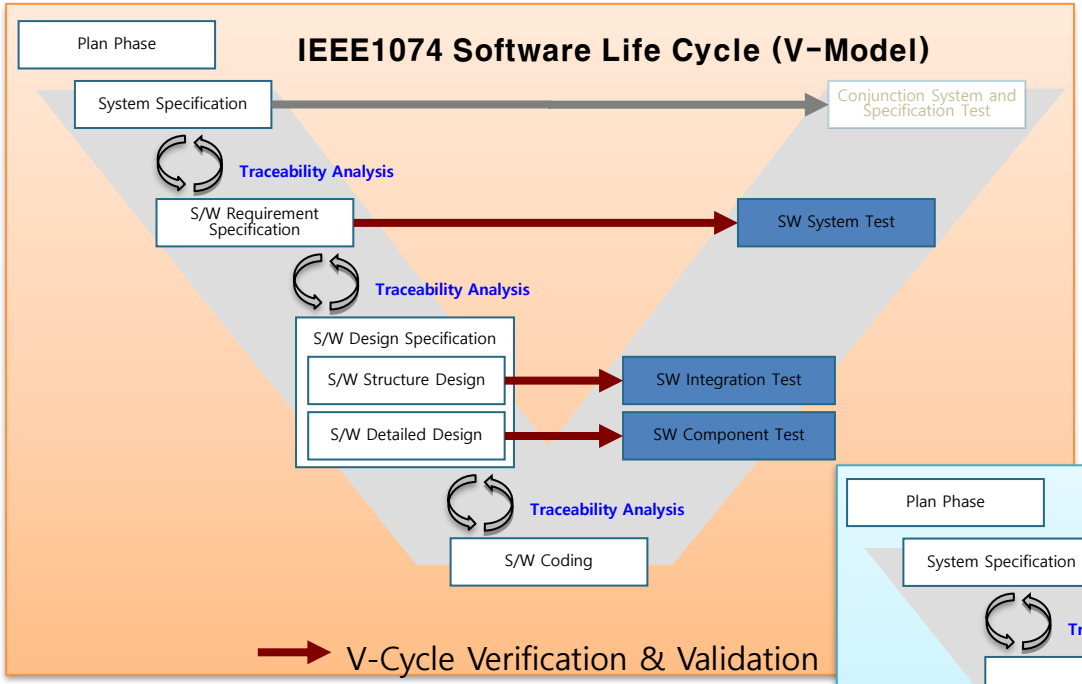
Integration(Board) Test

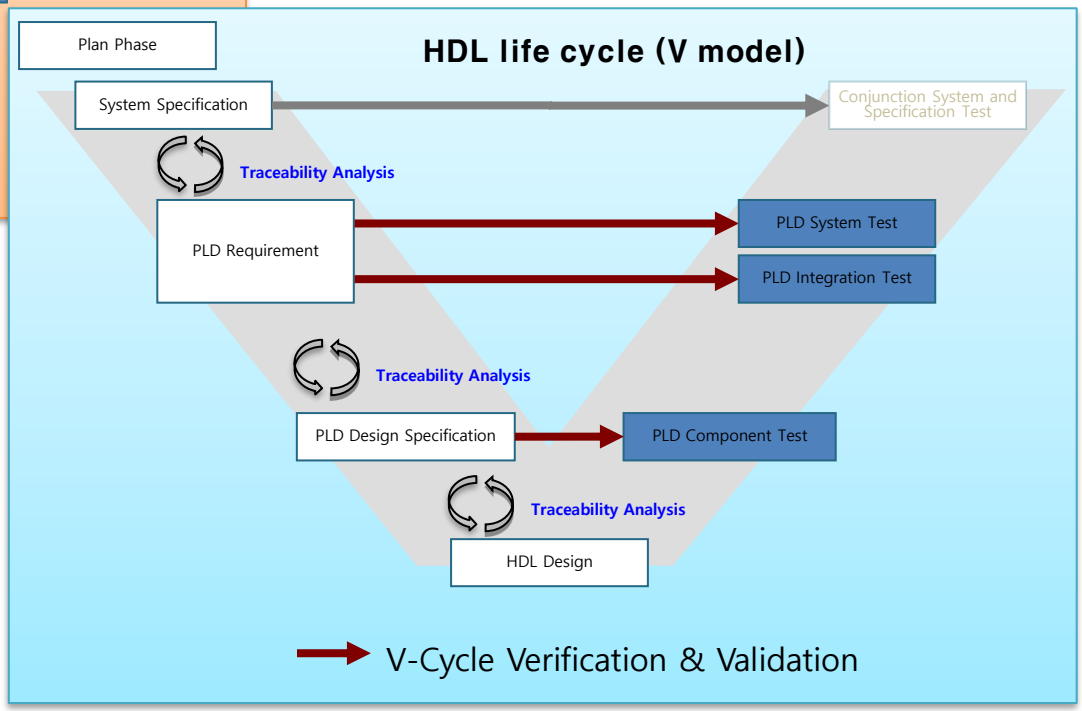
: After the download to FPGA final design has been completed and tested using the Logic Analyzer a signal at Board level.



PLD development using V-model

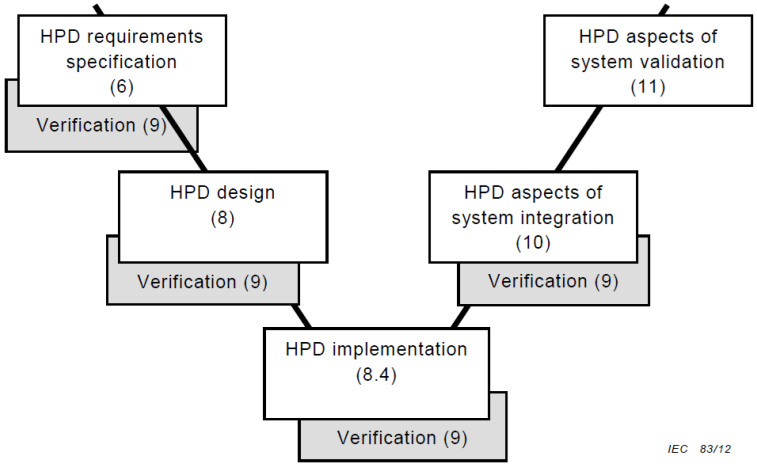
- HDL Life Cycle same as S/W Life Cycle





Life-Cycle of Codes & Standards

IEC 62566



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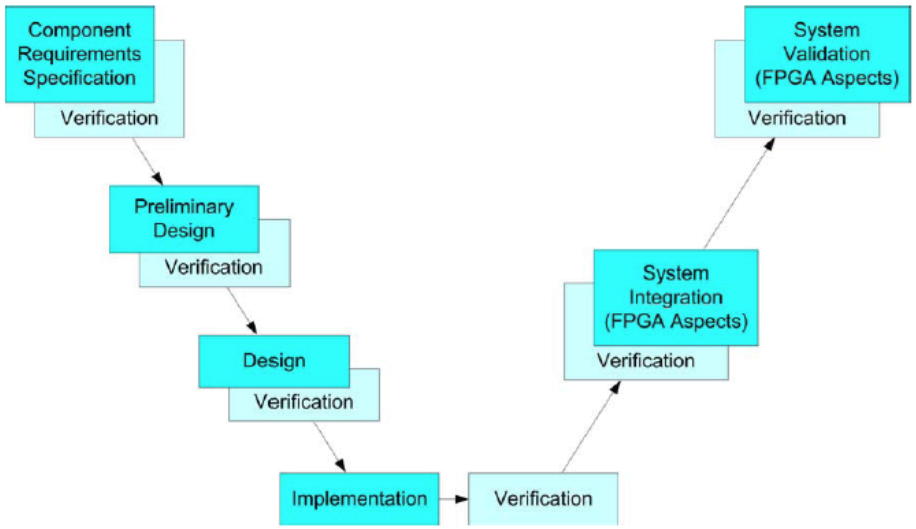
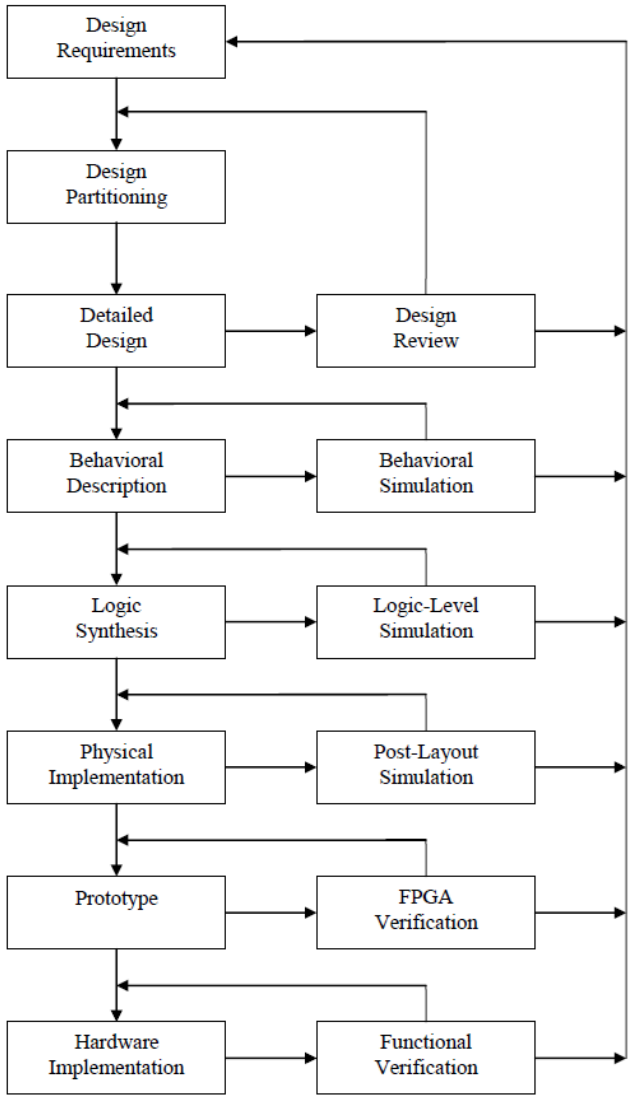
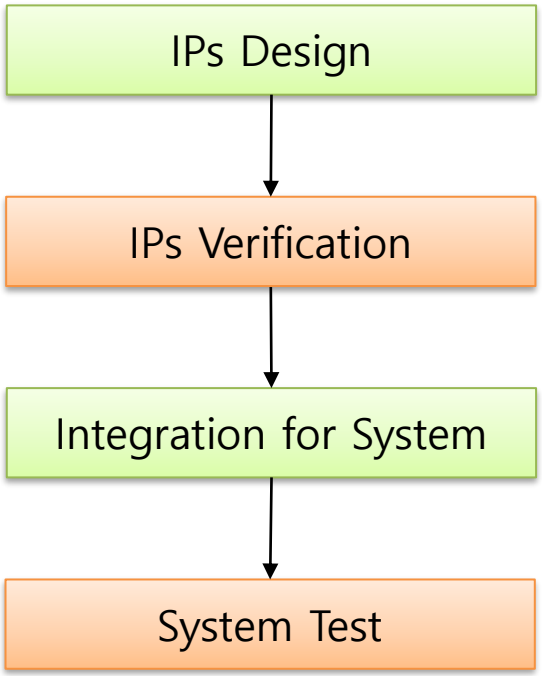


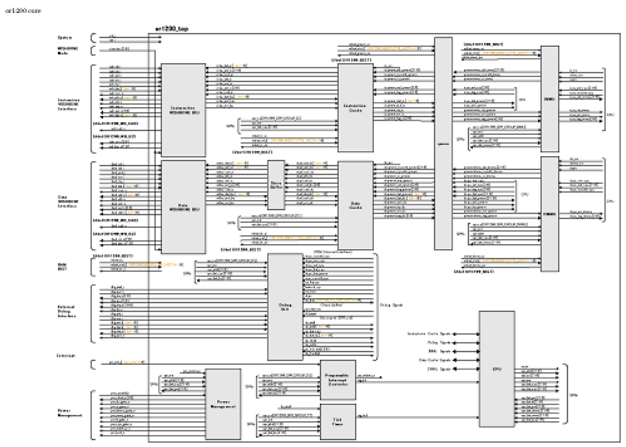
NUREG/CR-7006



Proposed Verification and Development Method

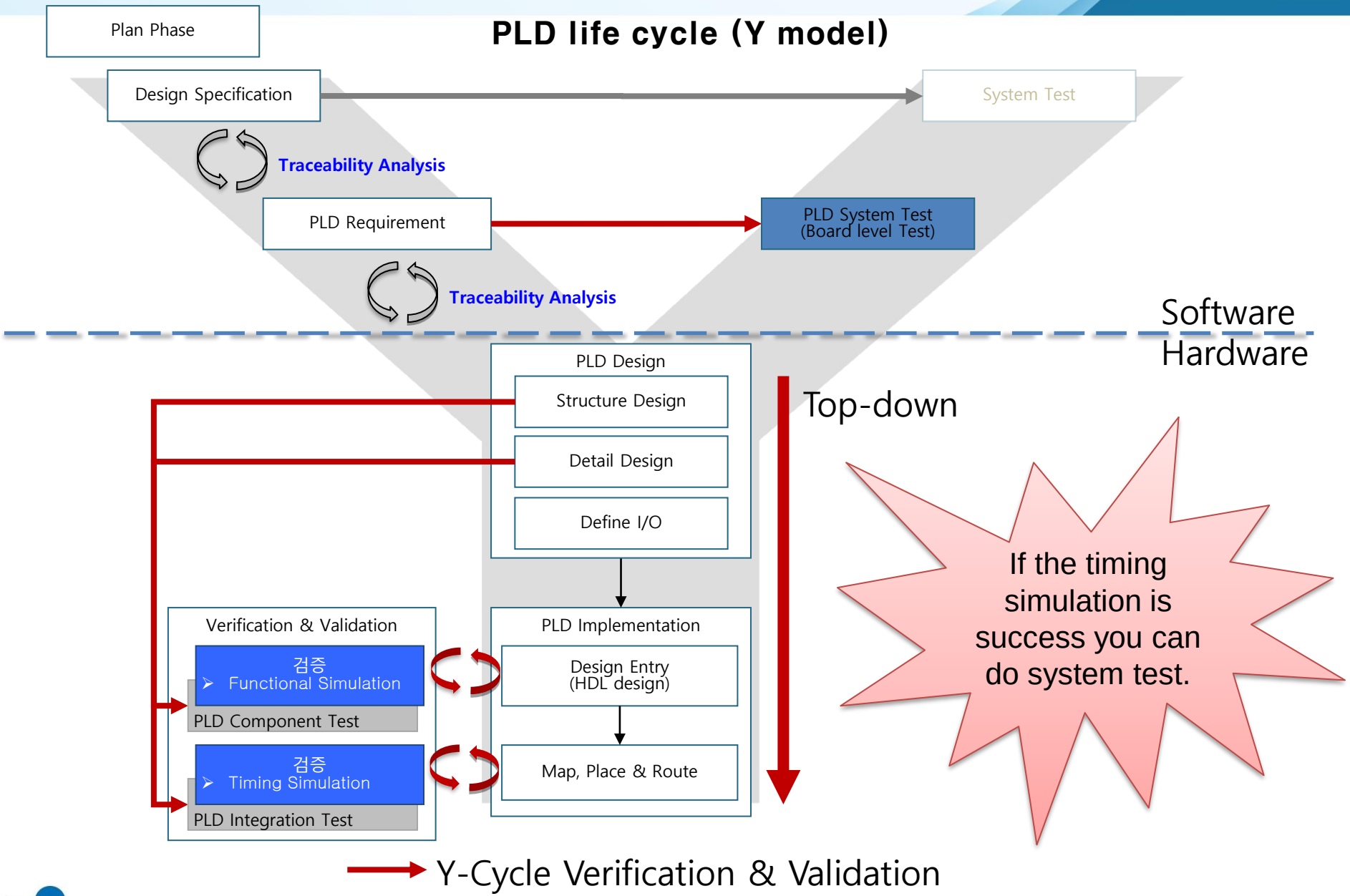


- The design IP (Intellectual Property) is how to develop SoC general.
- The V&V (Verification and Validation) for the IP of each, how to develop and validate the proposed increase the reliability of the features of IP.
- It is a method to perform the function of a FPGA making the Top-module which is combination of thus made the IPs.



- It is necessary to analyze the exact system requirements, the division of each Component specific features you must clear.
- Verification of IP, which is divided each function, is performed timing, implementation and test.

Recommend Life-Cycle (Y-model)



Conclusion

- In developing the FPGA in the V-model, which was provided for software development, has seen a number of limitations on the development of hardware-based FPGA.
- The item designed to HDL has been verified a viewpoint of software.
- Verification is the middle viewpoint between hardware and software after P&R.
- After the actual downloaded to the FPGA, in hardware verification Board level.
- It is possible to complement the V-model that was developed showing the limits on the FPGA, in fact, I propose a method can be designed to suit the FPGA.

THANK YOU

PONU-Tech Co., Ltd.