Verification of Hardware for Eddy Current Testing System

Sung-Nam Choi [a*], Hee-Jong Lee , Seung-Ok Yang
[a] *System Engineering Lab., Korea Hydro & Nuclear Power-Central Research Institute, 70, 1312 bun-gil, Yusung dae-ro, Yusung-gu, Daejeon 305-343, Korea*
[*] *Corresponding author: snchoi@khnp.co.kr*

1. Introduction

Nondestructive testing (NDT) for the construction and operating of NPPs plays an important role in confirming the integrity of the NPPs. Especially, Eddy current testing (ECT) is one of the primary nondestructive examination methods for in-service inspection of the tubes in major components in NPPs.

Korea Hydro & Nuclear Power-Central Research Institute (KHNP-CRI) has developed an eddy current testing (ECT) hardware (H/W) consisted of synthesizer, receiver, AD converter, FPGA (Field Programmable Gate Array) and processor unit.

During the development of the ECT hardware, verification and validation of design is required in order to prevent errors and reduce cost. The printed circuit board (PCB) of ECT hardware was verified with simulation in order to configure prescribed performance.

This paper gives an overview of the evaluating and applying FPGA-based PCB in the ECT HW system.

2. Simulation of ECT Hardware System

Main steps in the design process and methods for FPGA (Field Programmable Gate Array) are followed; requirements definition, HDL(High Description Language) programming, simulation using HDL, synthesis, simulation using the netlist, place and route, simulation based on place and route (P & R) output, implementation and testing on a test board.

Main FPGA and AD converter of ECT system shows in Fig. 1.

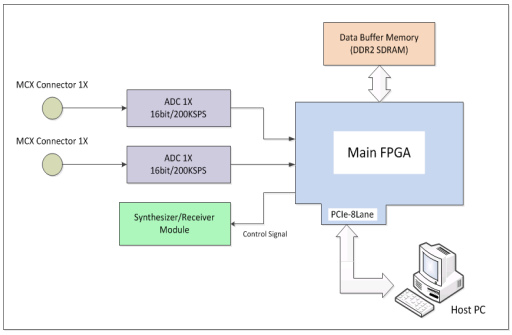

Fig. 1 Main FPGA and AD of ECT system

According to DO-254 (Design Assurance Guidance for Airborne Electronic Hardware) rule check, FPGA and PCB for the ECT HW system were verified. FPGA of the ECT HW was checked to readability and performance of code with ModelSim®. EMC (Elector Magnetic Compatibility) and EMI (Electro Magnetic Interference) of the PCB was checked with HDL Designer and Hyper Lynx to provide the assurance of the design.

2.1 Simulation of FPGA Verification

Coverage of FPGA code steps to make sure whether the RTL (Register Transfer Language) code is unnecessary or unproven.

Even though there are no errors in FPGA, RTL code has to be assured the all the action perfectly. Typically the input scenario was simulated with the test bench to work correctly. Coverage of the RTL code shows the percentages of the RTL code to be run. The coverage results for AD converter and synthesizer show that in Fig. 2.

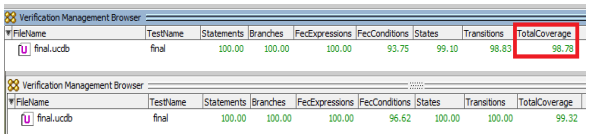

Fig. 2 Coverage for AD and synthesizer of ECT system

After the RTL code was checked with the coverage, DO-254 rule was checked. There were 238 errors with 9 rules in the AD convertor and 138 errors with 5 rules in the synthesizer. The errors occurred in the initialization of signal, the overlap of object's names and unused objects. The errors were removed from the revised RTL code.

Synthesis and P & R process was checked whether the behavior to match the frequency on the specification of ECT hardware. The result of synthesis for AD converter shows the speed of operating was up to 113.0 MHz based on 20MHz main clock and synthesizer shows the speed of operating was up to 59.9 MHz. The final results of all the FPGA show that the speed of operating ran faster than the specification.

2.2 Simulation of PCB Verification

The main issues of the PCB manufacturing technology is a low-power and high-speed switching. However, the use of a wide range of voltage and current and the reduced size of the PCB copper foil lead to increase noise due to the switching speed and fine process. According to the density of the wiring board, the complexity of design has gone up significantly compared to the past.

The board is designed by considering the integrity and manufacturing and checked the design process to be implemented in advance.

For the analysis of the signal integrity for PCB of the ECT HW, the impedance discontinuity, common and differential mode radiations were checked.

The threshold skew and multi cross were analyzed and showed the results in Fig. 2 to be converged over 1000 mV.

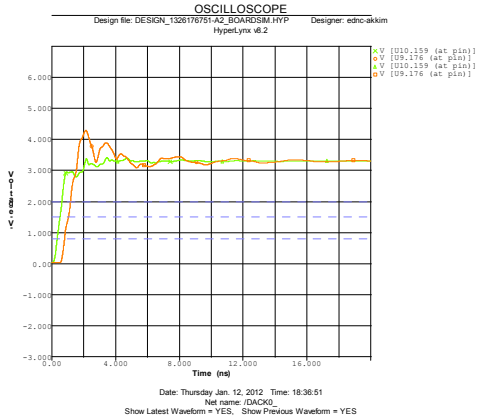

Fig. 2 The result of Signal Integrity analysis

For the analysis of EMC for the PCB to be operated normally and ensured stable product quality, the checklist of design was created.

The checklist is comprised of 3 parts. The checklist for EMC problems included edge shied, exposed length, nets crossing gaps, nets near plane edge and reference plane change. The checklist for the signal integrity included differential pair, guard trace, long nets/stub, many vias and loop area. The checklist for power integrity included decoupling capacitor placement, and power/ground width.

PCB of ECT HW was checked with the checklist and insured the margin of design requirements. The design of ECT HW modified and checked again not to violate the checklist.

The result of long net detection was in Fig. 3.

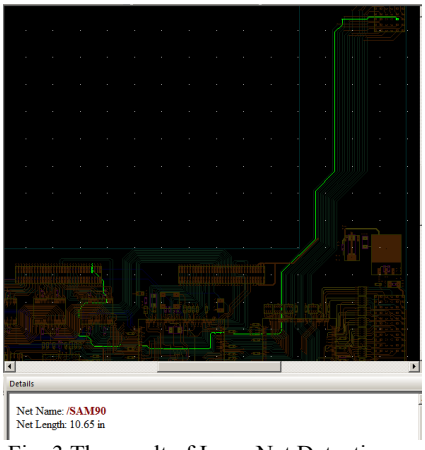

Fig. 3 The result of Long Net Detection

3. Conclusions

This paper gives an overview of the functional simulation of ECT HW for verification.

Before the implementation of PCB based on FPGA, the ECT HW was checked with simulation program and modified the design to operate correctly.

The simulation can be insured the integrity of the PCB and reduce time and cost of the manufacturing.

First of all, the simulation will enhance the quality and performance for the PCB based on FPGA.

The technologies related with the developed ECT HW will give a chance to develop other PCB in KHNP.

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