# Test Results of Event Timing System for KOMAC 100-MeV Proton Linac

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## 1. Introduction

The Korea multi-purpose accelerator complex (KOMAC) has two beam extraction points at 20 and 100 MeV for proton beam utilization [1]. A timing system is required to synchronize the KOMAC subsystems such as the ion source, the Low-Level Radio Frequency LLRF systems of the Radio Frequency Quadrupole RFQ and Drift Tube Linac (DTL), and the diagnostic devices. A timing signal for the beam extraction and diagnostic should be controlled by referencing the synchronized timing information. As a KOMAC timing system, a pulse delay generator was limited to distribute the timing signals to be accurate and flexible, providing multiple outputs. It also has several drawbacks which are not synchronized with RF and AC main frequency. The timing system will be upgraded to the Micro Research Finland (MRF) event system. The event timing system has been tested with Event Generator (EVG) and Event Receiver (EVR) using Experimental Physics and Industrial Control System (EPICS) software [2]. In this paper, we will describe the design, implementation, and test results of new timing system.

## 2. Overview of Timing System

The KOMAC accelerator facility was designed to provide many users with the proton beams of various beam conditions. Representative specifications of the KOMAC linac are maximum beam energy of 100 MeV, peak beam current of 20 mA, and the adjustable repetition rate is up to 120 Hz.

The EVG is responsible for generating and sending out event codes over 2 Gbits/s fiber optic links to an array of EVR that is programmed to decode specific event codes. The EVR generates trigger signals for the beam, rf, and ac magnet power supply through the fan-out board. The event timing system for the KOMAC facility will be installed as shown in Fig. 1.

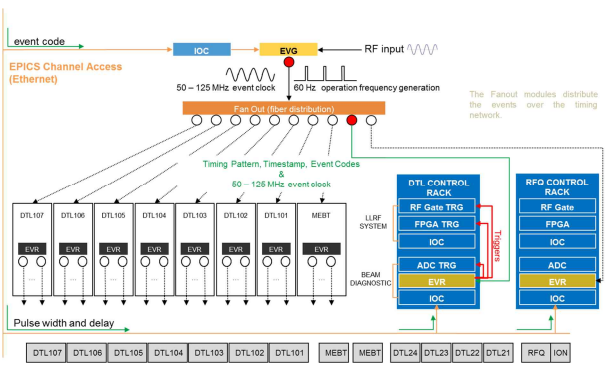


Fig. 1. Block diagram of the KOMAC timing system

## 3. System Configuration

### *3.1 Hardware*

The test system consists of a most simple setup to get the EVG and EVR pair working. Figure 2 shows the layout for a simple test of the event timing system.

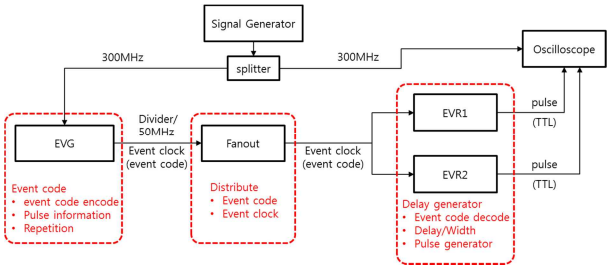


Fig. 2. Schematic layout for the event timing system

This setup is meant to get the EVG send out a simple signal that the EVR can put on the output, and if everything is fine the output phase should be locked to the RF input. The hardware configuration is shown in Fig. 3.

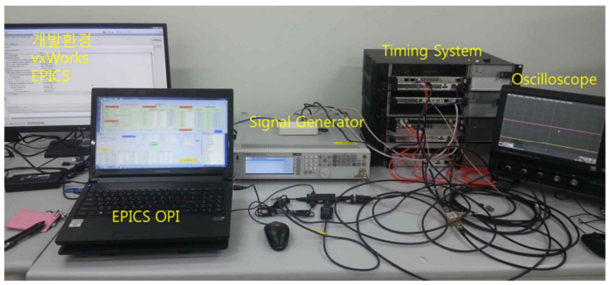


Fig. 3. Hardware setup of event timing system

The EVG creates and sends out timing events to an array of EVR as shown in Fig. 1. High configurability makes it feasible to build a whole timing system with a single EVG without external counters. Events are sent out by the EVG as event frames which consist of an eight bit event code and an eight bit distributed bus data byte. The event transfer rate is derived from an external RF clock. The optical event stream transmitted by the EVG is phase locked to the clock reference. The timing system will be tested to check the synchronization between the clock reference and output pulses using several sources of events such as trigger events, sequence events, and software events.

### *3.2 Applications*

EPICS can integrate the timing systems and other Input Output Controllers (IOC) supporting network

based real-time distributed control. The timing systems are connected by two network devices of a control network and a timing network. The device/drivers supported by application interface functions were modified to satisfy the operation mode. The device/driver support layer which mainly interacts with the registers mapped on the VME memory was developed with the event generator record and event receiver record of the event record. A Linux serves an integrated development environment for IOC and VXWORKS which is the operating system of the timing system. The Operator Interface (OPI) are implemented using Control System Studio (CSS) as shown in Fig. 4 and 5.

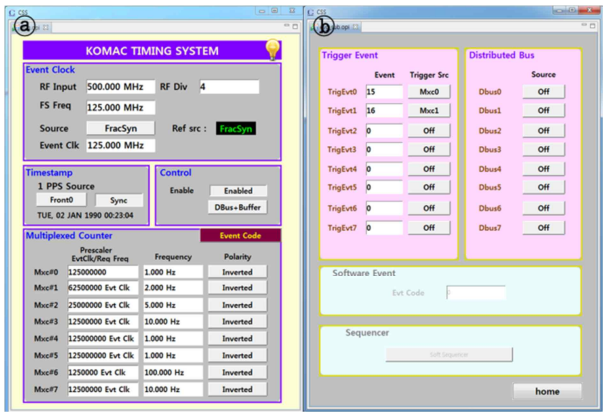


Fig. 4. OPI of event generator: ⓐ and ⓑ panels for setting RF clock and event code

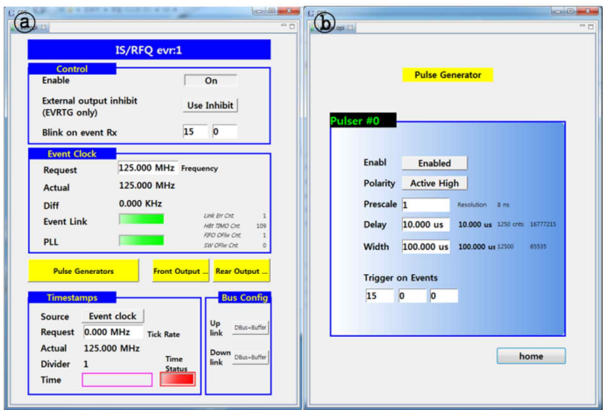


Fig. 5. OPI of event receiver: ⓐ and ⓑ panels for setting pulse output channel and pulse generator

## 4. Results

The hardware system was setup with trigger event modes which are created from event code bits. The first seven bits of an event code can be used to generate a trigger pulse directly. It is one of the simplest ways to use an event code. The output pulse is one event cycle long; in our case this means 20 ns. An easy way to make a trigger event is to use a divider in the EVG multiplexed counter. The test results show that one period of EVR2 matches 10 period of EVR1 (Fig. 6) and pulses of EVR matches 300MHz of the RF signal (Fig. 7).

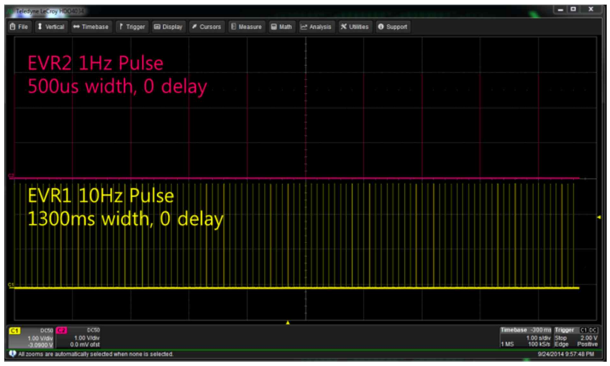


Fig. 6. Synchronized output pulses of EVR1 and EVR2 under different repetition rate.

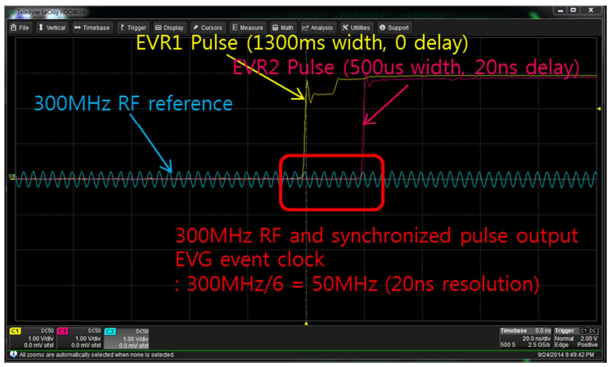


Fig. 7. Output signals of EVR1 pulse, EVR2 pulse, and 300MHz RF reference.

## 5. Conclusions

The timing system has been tested using EVG and EVR. The test results have shown that the output signals are synchronized between two EVRs and a RF reference. In the test, we have confirmed that each duty and delay of a pulse is able to be controlled by referencing the trigger event and the sequence RAM clock from the event generator. The event timing system will be installed and tested in summer maintenance period.

## ACKNOWLEDGMENT

This work was supported by the Ministry of Science, ICT & Future Planning of the Korean Government.

## REFERENCES

[1] Yong-Sub Cho, Hyeok-Jung Kwon, Dae-Il Kim, Han-Sung Kim, Jin-YeongRyu, Bum-Sik Park, Kyung-Tae Seol, Young-Gi Song, Sang-Pil Yun, Ji-Ho Jang, “The Komac Accelerator Facility”, Proceeding of International Particle Accelerator Conference, Shanghai, China, 2013.
[2] Experimental Physics and Industrial Control System (EPICS). URL:http://www.aps.anl.gov/epics.