Development of RF non-IQ sampling module for Helium RFQ LLRF system

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1. Introduction

KOMAC (Korea Multi-purpose Accelerator Complex) has a plan to develop the helium irradiation system. This system includes the Ion source, LEBT, RFQ, MEBT systems to transport helium particles to the target. Especially, the RFQ (Radio Frequency Quadrupole) system should receive the 200MHz RF within 1% amplitude error stability. For supplying stable 200MHz RF to the RFQ, the low-level radio frequency (LLRF) should be controlled by control system.

This LLRF control system adopted the commercial digital board using the FPGA (Field Programmable Gate Array). The specifications of a commercial digital board introduced in the Table 1.

Table 1. Specifications

ADC	Texas Instruments, ADS5474
	Sampling rate : 20 ~ 400MHz
	Resolution : 14bit
DAC	Texas Instruments, DAC5688
	Input data rate : 250MHz max.
	Output IF : DC to 300MHz
	Resolution : 16bit
FPGA	Two xilinx virtex-5

The helium RFQ LLRF control system adopted non-IQ sampling method to sample the analog input RF. Sampled input data will be calculated to get the I, Q values. These I, Q values will be used to monitor the amplitude and phase of the RF signal. In this paper, non-IQ sampling logic and amplitude & phase calculating logic of the FPGA will be introduced.

2. System layout & Module design

The helium RFQ RF system layout is shown in Fig. 1.

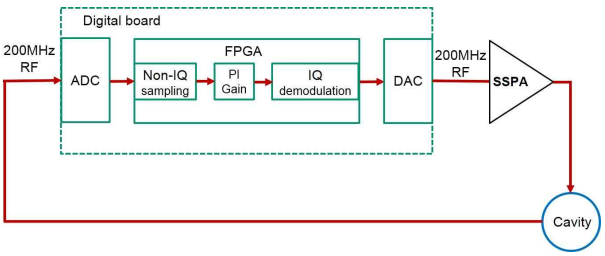

Fig. 1. Helium RFQ RF system layout

Before the LLRF is amplified by the 240kW SSPA (Solid-State Power Amplifier), the LLRF should be controlled by the control system because the SSPA does not control the input RF signal but just amplifies the input RF signal. The FPGA installed in the LLRF control board will compute and tune the sampled digital data that received from ADC chip. Then the FPGA transfers computed I, Q values to the DAC chip to make the controlled LLRF signal that amplified by the SSPA. This FPGA control logic layout is shown in Fig. 2.[1]

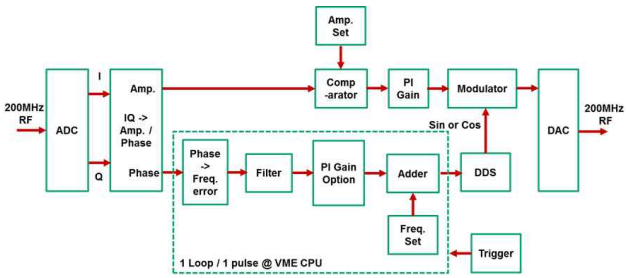

Fig. 2. The FPGA control logic layout

The designed FPGA control logic will be developed module by module.

2.1 Module-1. non-IQ sampling

First, the ADC chip directly samples the input RF signal using non-IQ sampling method. In the helium RFQ LLRF system case, 5(=N) samples sampled per 3(=M) periods. As a result, the digital data will be sampled per 3ns. This module computes the sampled digital data to make the I, Q values per 3ns. To develop the non-IQ sampling module, the Equation (1) should be computed in the FPGA as a logic. This equation implemented using FIR (Finite Impulse Response) filter in the FPGA. In the Equation (1), N means 5, y_i means sampled digital data. Also, the sine & cosine terms mean the coefficient.

$$I = \frac{2}{N} \cdot \sum_{i=0}^{N-1} y_i \cdot \sin(i \cdot \Delta\Phi)$$
$$Q = \frac{2}{N} \cdot \sum_{i=0}^{N-1} y_i \cdot \cos(i \cdot \Delta\Phi), \quad \Delta\Phi = 2\pi \cdot \left(\frac{M}{N}\right) \quad (1)$$

Equation (1). I, Q values solved by applying least mean square algorithm

The FIR filter implemented as shown in Fig. 3. The input data of this filter is non-IQ sampling digital data

and the out data of this filter is computed I value or Q value.

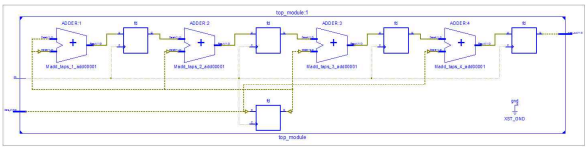

Fig. 3. Implement of the FIR filter in the FPGA

2.2 Module-2. Amplitude_phase

This module calculates the amplitude and phase of the input RF signal. The computed I, Q values of the module-1 are input data of the module-2. The module-2 implements Equation (2) to compute the amplitude and phase.[2]

$$Amplitude = \sqrt{I^2 + Q^2}$$
$$Phase = \arctan\left(\frac{Q}{I}\right) \quad (2)$$

Equation (2). Amplitude and phase values solved using I, Q values

Equation 2 is implemented in the FPGA with the CORDIC IP core. After amplitude and phase calculated, these values are transferred to the EPICS for monitoring. The implemented amplitude and phase computing module design is shown in Fig. 4.

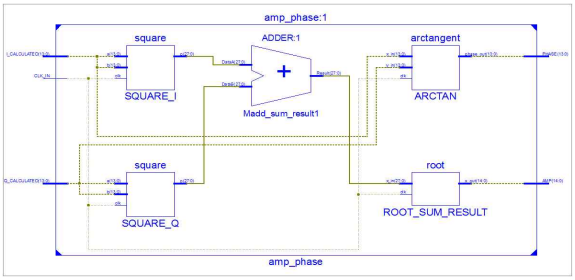

Fig. 4. Implement of the module-2 in the FPGA

3. Simulation results

3.1 Module-1 simulation result

Fig. 5 shows the simulation result of the module-1. The analysis of the Fig. 5 explained in Table 2. The sampling clock period is 3ns and the digital data inputted to the module-1 per 3ns.

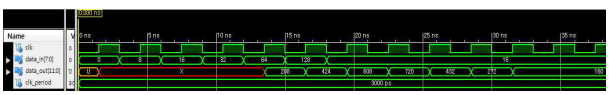

Fig. 5. Simulation result of the module-1

Input data	Coefficient	Output data
x[0] = 0	h[0] = 1	y[0] = 208
x[1] = 8	h[1] = 2	y[1] = 424
x[2] = 16	h[2] = 4	y[2] = 608
x[3] = 32	h[3] = 2	y[3] = 720
x[4] = 64	h[4] = 1	y[4] = 432
x[5] = 128		y[5] = 272
x[6] = 16		y[6] = 160

Table 2. The analysis of the Fig. 5

3.2 Module-2 simulation result

The Fig. 6 shows the simulation result of the module-2. The analysis of the Fig. 6 explained in the Table 3. The sampling clock, I value, Q value inputted to the module-2 per 3ns.

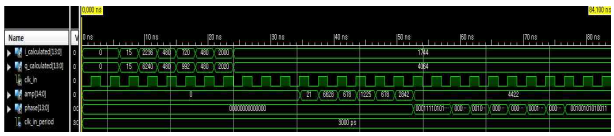

Fig. 6. Simulation result of the module-2

I value	Q value	Amp.	Amp. Simulation result	Phase [rad]	Phase simulation result [Binary floating-point]
15	15	21.213	21	0.7853981	00011001001010
2236	6240	6628.521	6628	1.2267169	00100111010000
480	480	678.822	678	0.7853981	00011001001000
720	992	1225.750	1225	0.9429597	00011110001011
480	480	678.822	678	0.7853981	00011001001000
2000	2020	2842.604	2842	0.7903732	00011001010010
1744	4064	4422.401	4422	1.1654294	00100101010011

Table 3. The analysis of the Fig. 6

4. Summary & Future works

Using Xilinx ISE design suite which is tool for developing the FPGA logic module, non-IQ sampling module and amplitude & phase computing module developed.

In the future, PI gain module and frequency error computing module will be developed. This future works will make possible for the helium RFQ LLRF control system to conduct the feedback control.

ACKNOWLEDGMENT

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