Implementation of FPGA-Based Diverse Protection System

Soo Yun Hwang *, Yoon Hee Lee, Se Do Shon, Seung Min Baek
KEPCO Engineering and Construction Company Inc., 989-113 Daedeokdaero Yuseong-gu, Daejeon, 305-353, Korea
**Corresponding author: syhwang@kepco-enc.com*

1. Introduction

It is well known that existing nuclear power plant (NPP) hardware platforms contain many components that are becoming obsolete at an increasing rate. Various studies have been conducted to address hardware platform obsolescence [1]. Obsolete analog and digital hardware platforms in NPPs are commonly replaced with programmable logic controller (PLC) and distributed control system (DCS).

Field programmable gate arrays (FPGAs) are highlighted as an alternative to obsolete hardware platforms. FPGAs are digital integrated circuits (ICs) that contain the configurable (programmable) blocks of logic along with configurable interconnections among these blocks. Designers can configure (program) such devices to perform a tremendous variety of tasks. FPGAs have been evolved from the technology of programmable logic device (PLD). Nowadays, they can contain millions of logic gates by nanotechnology and can be used to implement extremely large and complex functions that previously could be realized only using application specific integrated circuits (ASICs) [2].

This paper presents the implementation of an FPGA-based diverse protection system (DPS) which executes the protective functions in NPP when the protective functions of the plant protection system (PPS) fails. The functional simulation of an application program for DPS is performed to verify its function using Modelsim. Application program logic was implemented with synthesizable register transfer level (RTL) very high speed integrated circuit hardware description language (VHDL) targeting Actel ProASIC3 FPGA and the Libero IDE v9.1 vendor development tool is used to perform the synthesis and placement & routing (P&R).

2. FPGA-Based Diverse Protection System

2.1 Basic Function

The DPS is composed of two channels. The DPS continuously monitors selected parameters to determine if a reactor trip or a safeguard initiation is required. The DPS receives measurements of selected parameters. There is a comparator per each parameter. The comparator compares converted digital value against a predetermined value to determine whether or not the sensed parameter has exceeded the setpoint value. Finally, the DPS decides a reactor trip or a safeguard initiation signal using 2-out-of-2 coincidence logic. The results of the comparators and coincidence logic are transmitted to maintenance and test panel (MTP).

2.2 Physical Description of FPGA-based DPS

The FPGA-based DPS rack assembly for one channel consists of logic processing module (LPM), analog input module (AIM), analog output module (AOM), digital input module (DIM), digital output module (DOM), and power supply module (PSM) as shown in Figure 1. It also contains a backplane that provides for distribution of power and for data signal transmission among the modules. Each module does not contain any traditional CPUs or OSs.

LPM1	LPM2	AIM	AOM	DIM	DOM1	DOM2	DOM3	DOM4	DOM5	PSM1	PSM2

Fig. 1. Configuration of FPGA-based DPS rack assembly.

The LPM collects input data from input modules, executes application program logic of DPS, and updates the value which drives the output modules. The DPS rack assembly has redundant LPMs. The loss of any single LPM does not degrade the ability of the DPS to perform its functions. In addition, the LPM includes the communication function which provides inter-communication between the DPS rack assembly and the MTP computer via RS-422 serial port.

The AIM reads and digitizes analog input signals and then transmits the digitized values to the LPM through the backplane. The AOM receives digitized values from the LPM through the backplane and converts them to analog output signals. The DIM reads and digitizes contact status and then transmits the digitized values to the LPM through the backplane. The DOM receives digitized values from the LPM through the backplane and converts them to contacts status.

The PSM provides DC power to the DPS rack assembly through the backplane. The PSM for the DPS rack assembly is redundant. The failure of one PSM does not impact the operation of the DPS rack assembly.

3. Application Program Logic for DPS

The protective function of the DPS is performed by application program logic. Figure 2 shows the overall structure of application program logic for the DPS.

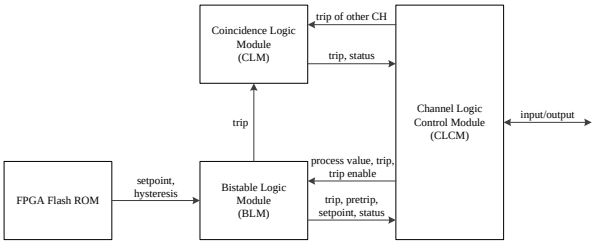

Fig. 2. Overall structure of application program logic.

The application program logic consists of flash ROM, coincidence logic module (CLM), bistable logic module (BLM), and channel logic control module (CLCM).

The setpoint and hysteresis for trip and pretrip of the DPS parameters are stored in FPGA flash ROM. The setpoint and hysteresis cannot be changed through MTP in FPGA-based DPS. The setpoint and hysteresis can be changed only through JTAG cable using the Libero IDE v9.1 vendor development tool.

The CLCM performs the input and output functions between the application program logic and other modules and controls the data flows for DPS functions.

The BLM includes the comparators which determine the trip and pretrip status of DPS parameters. There is a comparator per each parameter. The comparator compares converted digital value with a predefined value to determine whether or not the sensed parameter has exceeded. There are six parameters in the DPS: pressurizer pressure (PZRP), containment pressure (CNMTP), steam generator 1 level (SG1L), steam generator 2 level (SG2L), turbine trip (TT), and manual trip (MT). The bistable logic for PZRP and CNMTP (SG1L and SG2L) is based on the rising (falling) trip bistable logic with fixed setpoint. The bistable logic for TT and MT is based on the binary trip bistable logic.

The CLM finally determines a reactor trip based on the trip signals of PZRP, CNMTP, TT, and MT and a safeguard initiation based on the trip signals of SG1L and SG2L, using 2-out-of-2 coincidence logic between 2 channels of the DPS.

4. Implementation Results of Application Program Logic for DPS

The application program logic for the DPS was implemented with a synthesizable RTL VHDL targeting an Actel ProASIC3 FPGA (A3P1000-256FBGA) and the Libero IDE v9.1 vendor development tool [3] is used to measure the area occupation ratio and clock period on FPGA.

Table I shows the experimental results. In Table I, the core means the basic unit of area in Actel FPGA. By virtue of Table I, we identified that the physical requirements for FPGA are satisfied.

Table I: Experimental results

Measurement Items	Results
Occupation Ratio of Core	63.81%
Occupation Ratio of IO	25.99%
Occupation Ratio of RAM/FIFO	12.50%
Occupation Ratio of FlashROM	100%
Clock Period	40.725MHz

In addition, the Modelsim SE simulator v10.0d [4] is used to perform the functional simulations. Figure 3 shows a part of the simulation results. By the simulation results, we verified that the functional requirements for the DPS are satisfied.

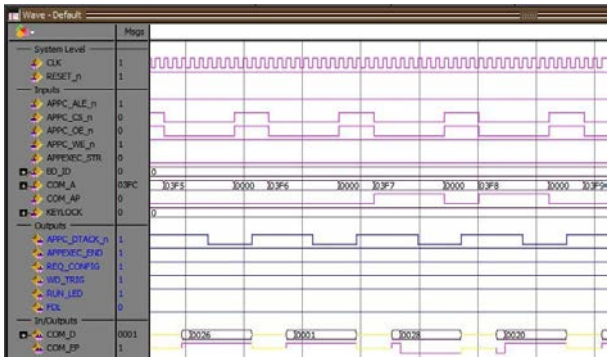

Fig. 3. Waveform view for the simulation results.

5. Conclusions

In this paper, we proposed the implementation of an FPGA-based DPS that executes the protective functions when the protective functions of the PPS fails in NPP. There are no CPUs and OSs in FPGA-based DPS rack assembly. Therefore, FPGA-based DPS has the diverse platform compared with the PPS based on CPUs and OSs. Experimental results show that the physical and functional requirements of the application program logic which performs the protective functions of DPS are all satisfied. We expect that the FPGA-based platform can be applied to other hardware platforms of NPP.

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