Simulation of the Direct Digital Synthesis module for Helium RFQ LLRF system

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1. Introduction

KOMAC (Korea Multi-purpose Accelerator Complex) has a plan to develop the helium irradiation system. This system includes the Ion source, LEBT, RFQ, MEBT systems to transport helium particles to the target. Especially, the RFQ (Radio Frequency Quadrupole) system should receive the 200 MHz RF within 1% amplitude error stability. For supplying stable 200 MHz RF to the RFQ, the LLRF (low-level radio frequency) should be controlled by control system.

This helium RFQ LLRF control system have a concept to track the cavity resonance frequency. For tracking the cavity resonance frequency, the FPGA (Field Programmable Gate Array) in the digital board will tune the frequency of the output sinusoidal signal.

In order to implement this frequency tracking concept, the DDS (Direct Digital Synthesis) module should be implemented in the FPGA.

In this paper, the DDS module in the FPGA simulated and the analysis result will be introduced.

2. System layout & Module simulation

The FPGA control logic of the helium RFQ LLRF system layout is shown in Fig. 1.



Fig. 1. Helium RFQ RF system layout

As shown in Fig. 1, the DDS module supply the sinusoidal digital data to the modulator. This digital data is 200 MHz frequency and DAC output frequency depends on the DDS output frequency.

2.1 Fundamentals of the DDS

Direct digital synthesis (DDS) is a technique for using digital data processing blocks as a means to generate a frequency- and phase-tunable output signal referenced to a fixed-frequency precision clock source. In essence, the reference clock frequency is "divided down" in a DDS architecture by the scaling factor set forth in a programmable binary tuning word. The tuning word is typically 24-48 bits long which enables a DDS implementation to provide superior output frequency tuning resolution.



Fig. 2. Frequency tunable DDS system

As shown in Fig. 2, the frequency tunable DDS system for frequency tracking of LLRF system have the three variables. The relationship between three variables and the output frequency is shown in Eq. 1.

$$f_o = \frac{M \times f_c}{2^N}$$

In order to track the resonance frequency, the tuning word M should be tune because system clock, N-bit carry fixed in the DDS system.

2.2 Frequency tracking method

The tuning word M should be preset to generate the 200 MHz basic output frequency. When the cavity changed under operation, tuning word M should be change immediately for applying the frequency error owing to the cavity change. The tuning word M following the Eq. 2 in the frequency tunable DDS system.

 $f_o = f_{pre_set} + \Delta f = \frac{M \times f_c}{2^N}$ f_{pre_set} : 200 MHz Δf : frequency error

Eq 2. Relationship between the tuning word and frequency error

2.3 DDS simulation

The DDS module simulation result in the FPGA shown in the Fig. 3. This result obtained using ISIM simulator. The reference clock is 500 MHz and 16 bit carry are fixed variables.

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Fig. 3. Simulation result of the DDS

3. Simulation result analysis

The digitized sinusoidal data of the Fig. 3 graphed in the Fig. 4 using EXCEL program. The sine, cosine digital data show the frequency change according to the tuning word M as shown in Table. 1.



the tuning word

Tuning word M	The output frequency
16384	125 MHz
10107.0	100 MIL
13107.2	100 MHz
9830.4	75 MHz

Table. 1. Relationship between tuning word and output frequency

4. Summary & Future works

Using Xilinx ISE design suite which is tool for developing the FPGA logic module, DDS module simulated.

In the future, frequency tracking system will be tested using test cavity. This future works will make possible for the helium RFQ LLRF control system to conduct the feedback control and simplify the cooling system of the helium RFQ.

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REFERENCES

[1] H. J. Kwon, H. S. Kim, Y. S. Cho, K. T. Seol, Control of the RF system for the Helium RFQ, Transactions of Korean Nuclear Society Autumn Meeting, October 2014

[2] J.Branlard, B.Chase, E.Cullerton, P.Joireman, V.Tupikov, LLRF Design for the HINS-SRF Test Facility at Fermilab, LINAC2010, Tsukuba, Japan, MOP083

[3] A Technical Tutorial on Digital Signal Synthesis, ANALOG DEVICES