

Configuration and application of He RFQ LLRF control system based on EPICS

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1. Introduction

The Korea Multi-purpose Accelerator Complex (KOMAC) has developed a Helium Radio-Frequency Quadrupole (He RFQ). In He RFQ device, the high-power Radio-Frequency (RF) is very important because it is responsible for the stable delivery and efficient acceleration of the beam. Since that, the control system of high-power Radio-Frequency must be developed and this system is called LLRF control system. The LLRF control system required exquisite amplitude value that has $\pm 1\%$ error range. We need a precise remote control system for this reason [1]. This paper represents the configuration of LLRF control system in terms of software layers based on EPICS. Also, this paper explains the application of LLRF control system to test environment (hardware) and represents test result and suggests future work.

2. Test Environment

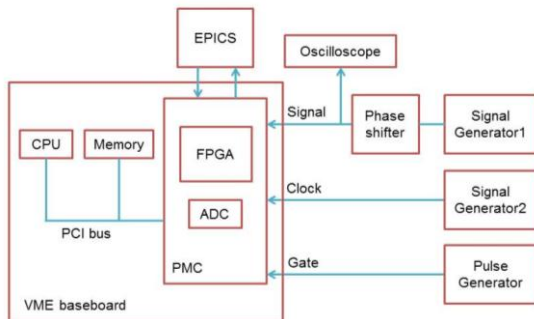


Fig. 1. Test environment block diagram

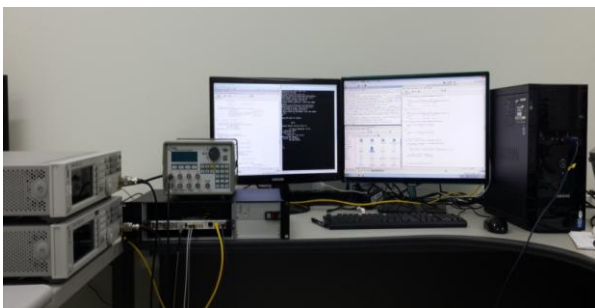


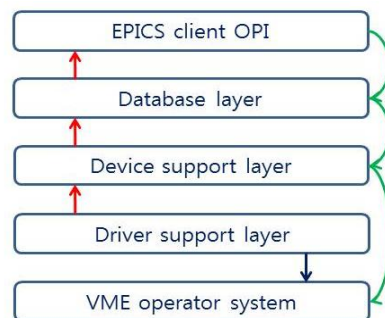
Fig. 2. LLRF control system test environment

Figure 1 shows the test environment block diagram. And figure 2 shows the real test environment. In terms

of hardware, IVME7210 baseboard and Pentek7156 FPGA PCI PMC extended board are selected. Because He RFQ uses a 200 MHz sampling rate, Pentek7156 is useful and selected. Figure 3 shows the VME SBC baseboard and FPGA PCI PMC extended board. VME SBC works as Experimental Physics and Industrial Control System (EPICS) Input Output Controller (IOC) [2]. In terms of software, figure 4 shows the EPICS software layers [3]. There is a driver support layer that configures the hardware modules. Above this, the device support layer makes the connection with EPICS through the database layer. EPICS is a standard software platform and provides a programming environment with an open source. In a client that remotes the LLRF system, Channel Access (CA) of the EPICS communication protocol through the Operator Interface (OPI) is used.



Fig. 3. IVME7210 baseboard and Pentek7156 FPGA PCI PMC extended board



← : Processed data which is stored in memory (data reading)

← : FPGA register WRITE function (data writing)

← : Initializing and configuring modules, Downloading object files to modules

Fig. 4. LLRF control system software layer based on EPICS

EPICS base 3.14.12.4 version is selected. And console program is used for configuration of VME SBC baseboard and vxworks operating system. Also, Pentek7156 board support package is selected for configuration of VME board [4].

3. Implementation

At first, we test the ADC module in VME SBC baseboard. ADC module converts the analog input signal to digital signal for mathematic calculation. Figure 5 shows the ADC module test result. The sampled data get from the ADC FIFO are stored in file. We show the data file in a graph.

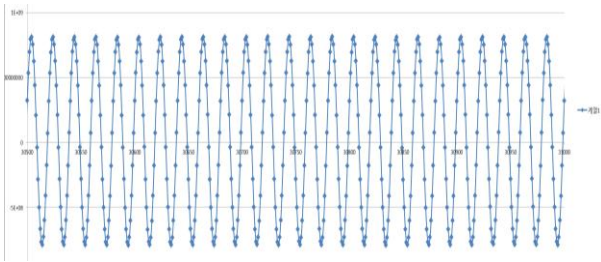


Fig. 5. ADC module test result

- Sampling frequency : 40 MHz
- Analog input to CH1 : 1 MHz, 0 dBm
- Gate signal : 1.7 ms, 1 Hz

After ADC module test, we test the DAC module and EPICS OPI communication test. DAC module converts the digital data to analog signal. Figure 6 show the analog output signal in oscilloscope.

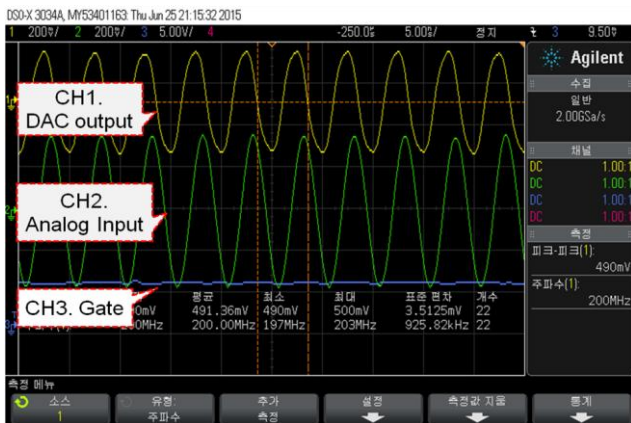


Fig. 6. DAC module test result

- Sampling frequency (DAC clock) : 400 MHz
- NCO frequency : 200 MHz
- DAC output frequency : 200 MHz

Figure 7 shows the real time data from console program and EPICS OPI client program. Client program read the real time data and write the set value to VME SBC baseboard.

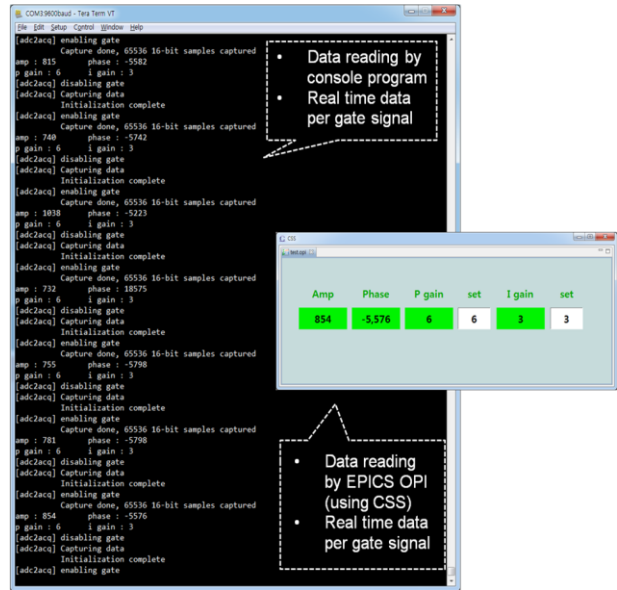


Fig. 7. EPICS OPI test result

4. Conclusions

The LLRF control system at the He RFQ is very important. The configuration of LLRF control system is completed on the software side and hardware modules: vxworks operating system installation, EPICS BASE compilation, module source code compiled, object file loading and execution on vxworks, EPICS IOC operation check, etc. The application of LLRF control system to module is implemented well: ADC module, DAC module, EPICS IOC test. In the future, test that switching sampling frequency and DAC output frequency is required with DDS and frequency tracking test is required with cavity. Also, floating the data in a graph is required and writing the data to FPGA will be improved.

ACKNOWLEDGMENT

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