사단법인 한국원자력학회
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KYUNG HEE UNIVERSITY

Design Verification Enhancement of FPGA-based PPS Trip Logics for Nuclear Power Plant

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Presented

By

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OUTLINES

1 *INTRODUCTION*

2 *METHODOLOGY*

3 *RESULTS*

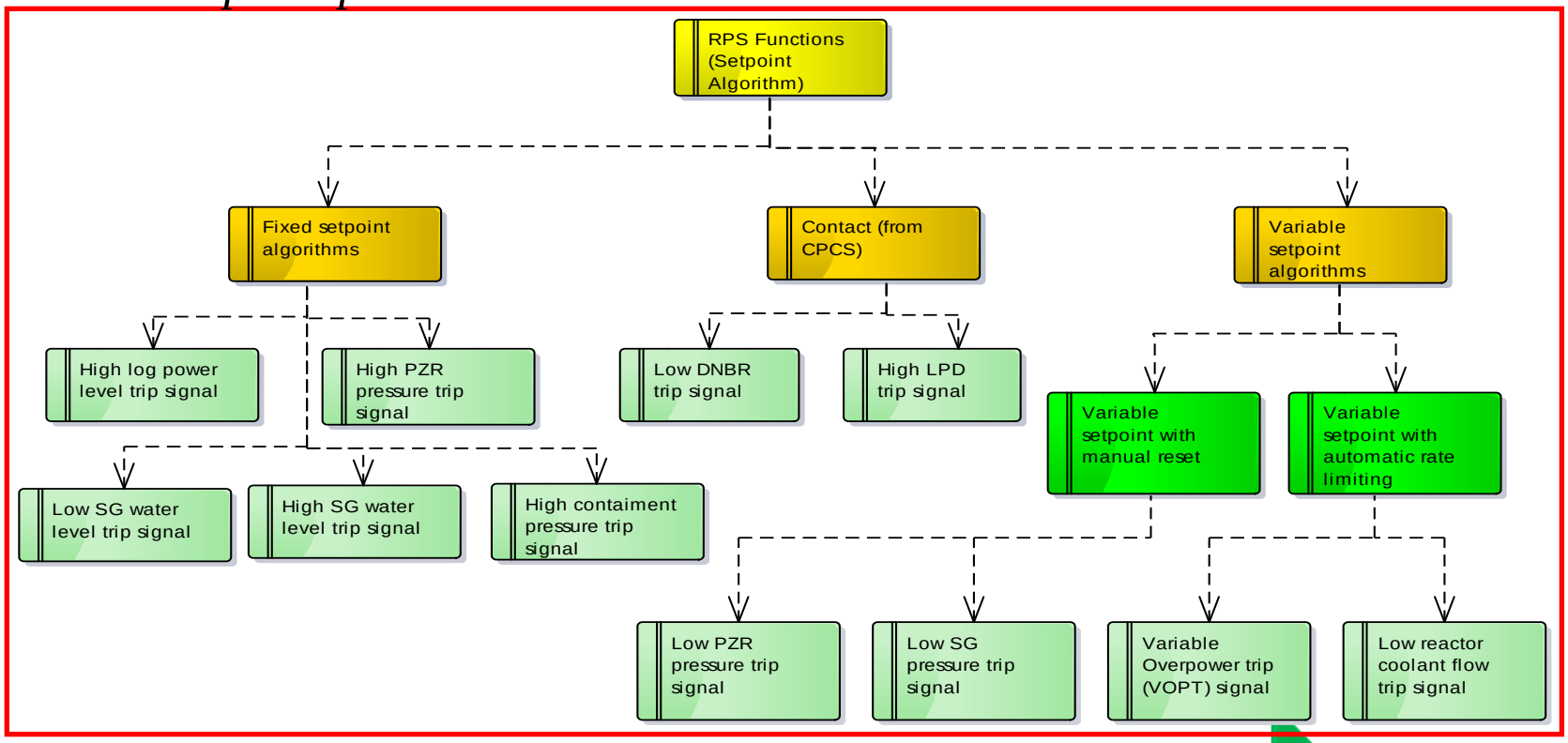
4 *CONCLUSIONS*

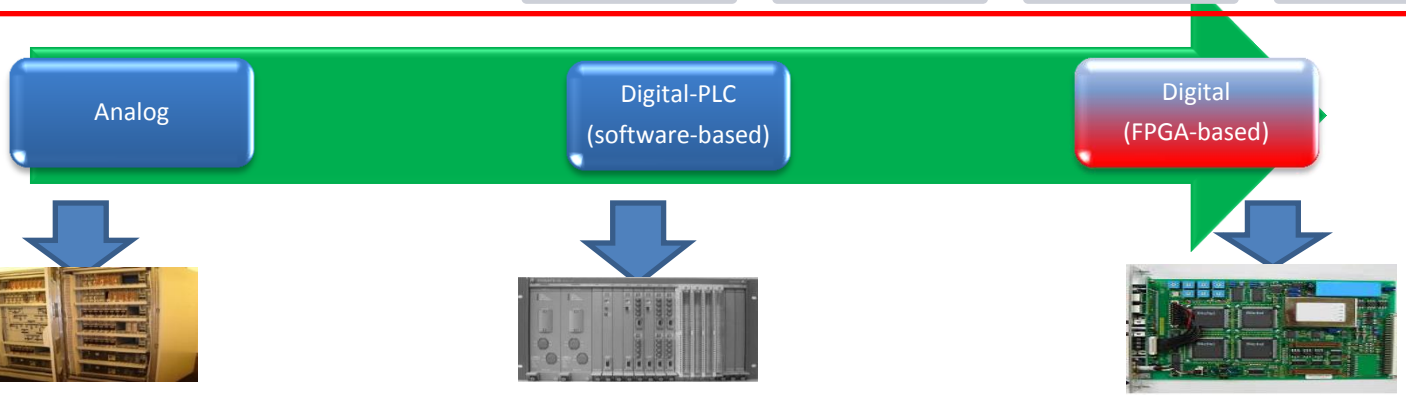
INTRODUCTION

- NPP (nuclear power plant) is design to have a safe plant operation throughout the plant design life time.
- Many safety systems are incorporated into NPP to achieve this crucial goal.
- Among these systems is I&C systems which coordinates the activities of the plant during normal and abnormal plant operation.
- I&C systems monitor, control and protect the activities and status of the plant condition, and making decisions base on the design.
- The safety critical part of I&C systems is plant protection system (PPS).
- The primary objective of PPS is to protect and provide a reliable and rapid reactor trip if monitored parameters approach the specified limiting setpoints.

INTRODUCTION

PPS plant parameters selected to be monitored.



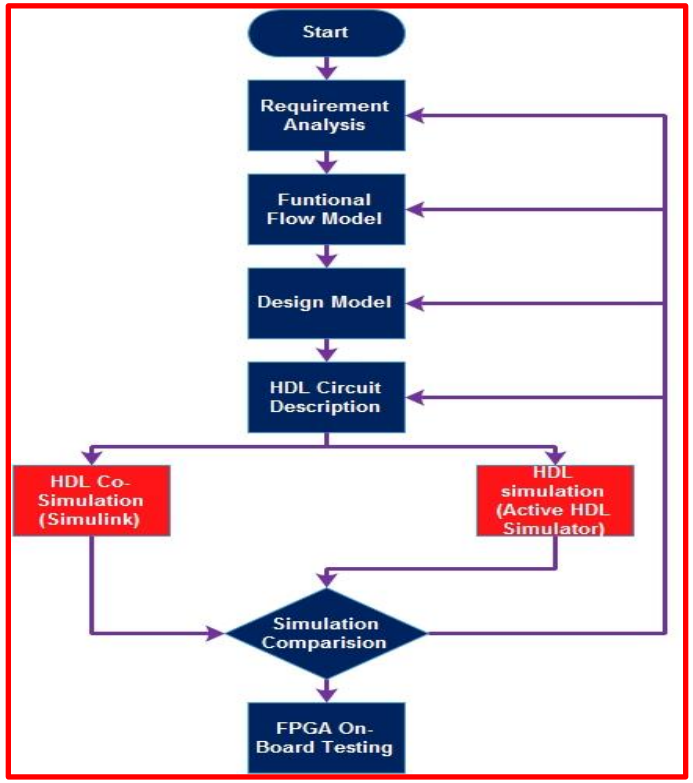


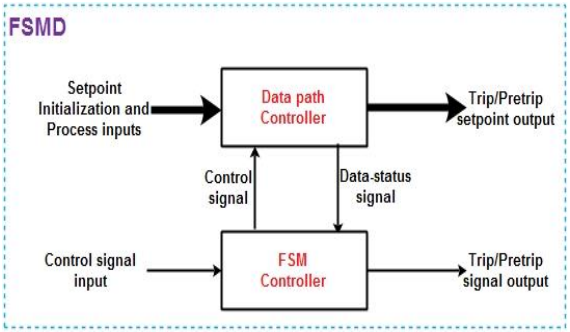
METHODOLOGY

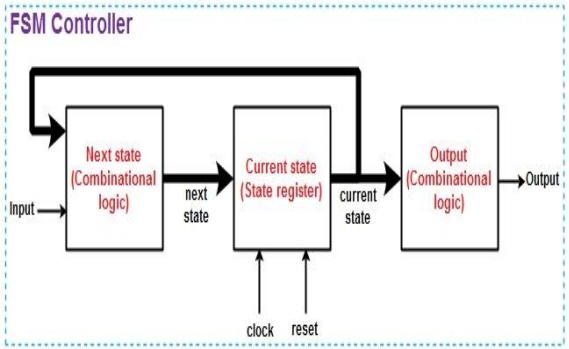
- *Research approaches*

Requirement analysis → Functionally model- EFFBD → Model design FSMD model (datapath + FSM) → VHDL circuit description codes development → Models verification → The verified model is validated and tested using Xilinx Spartan3E-100 CP132 FPGA board

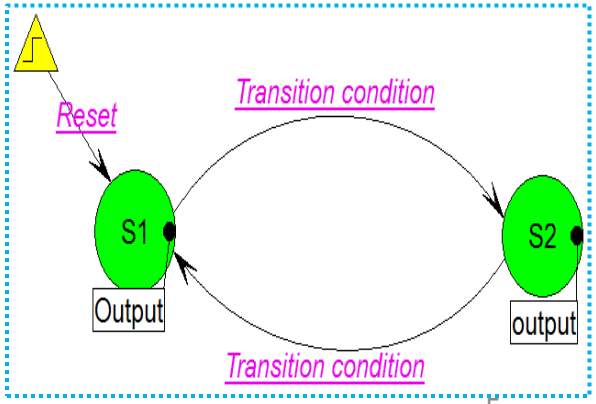
CORE™ ALDEC THE DESIGN VERIFICATION COMPANY MATLAB SIMULINK







DIGILENT BEYOND THEORY



METHODOLOGY

- ***Design Requirements***
  - ❖ ***Requirement - Regulations***

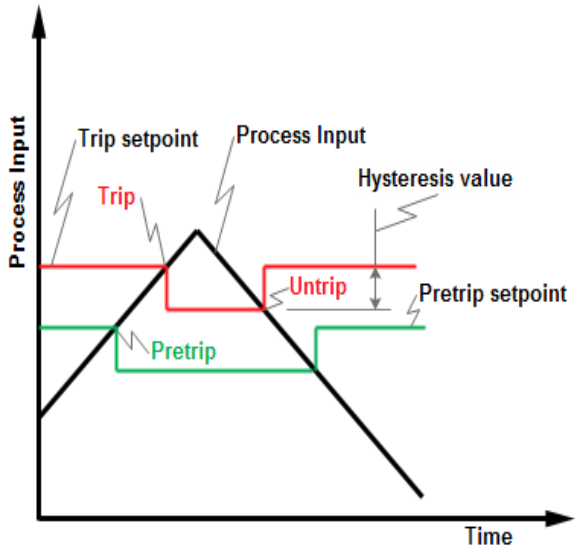
- **10CFR50 Appendix A**, GDCs 13, 20, 21, 22, 23
- **RG 1.152** – Criteria for Digital Computers in Safety Systems of Nuclear Power Plants
- **RG 1.153** – Criteria for Safety Systems

Standards

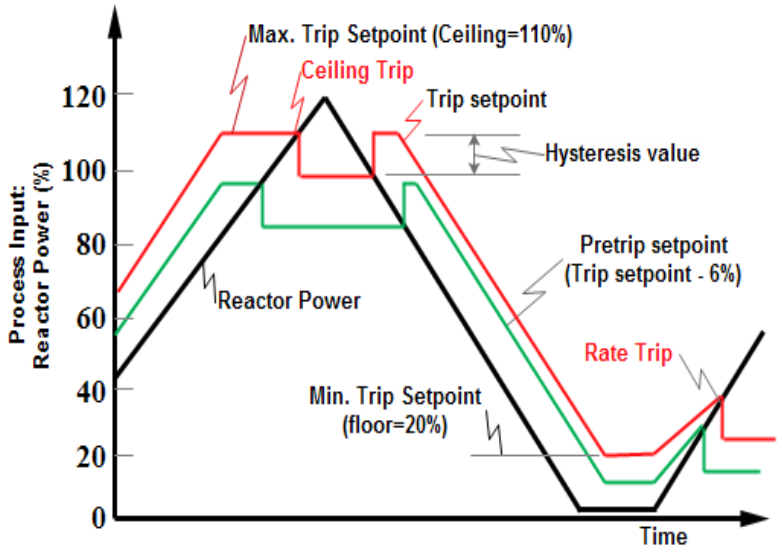
- **IEEE 7-4.3.2** - IEEE Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations
- **IEEE 603 1991** – Criteria for Safety Systems for Nuclear Power Generating Stations
- **IEC 62566** - Nuclear power plants – Instrumentation and control important to safety – Development of HDL-programmed integrated circuits for systems performing category A functions, 2012.

METHODOLOGY

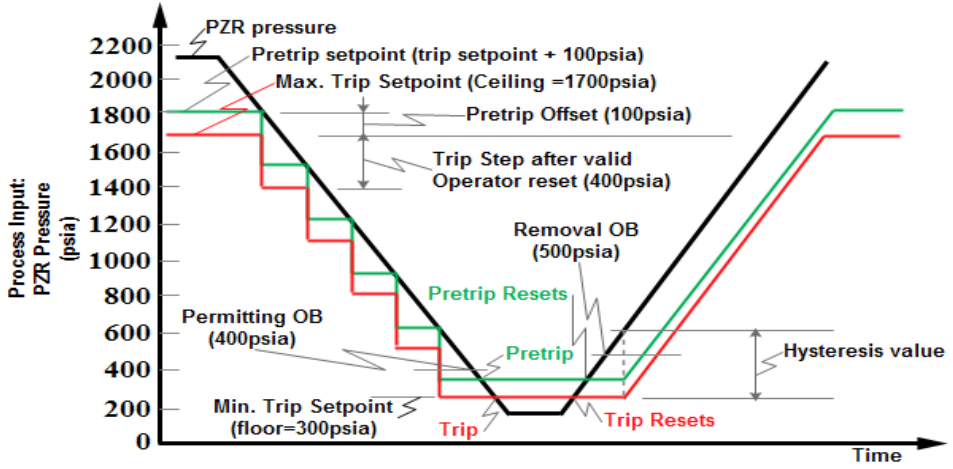
- ***Design Requirements***
  - ❖ ***Requirements – Functional***



(a) Bistable with Fixed Setpoint - Trip on increasing



(b) Bistable with Variable Rate limiting Setpoint - Trip on

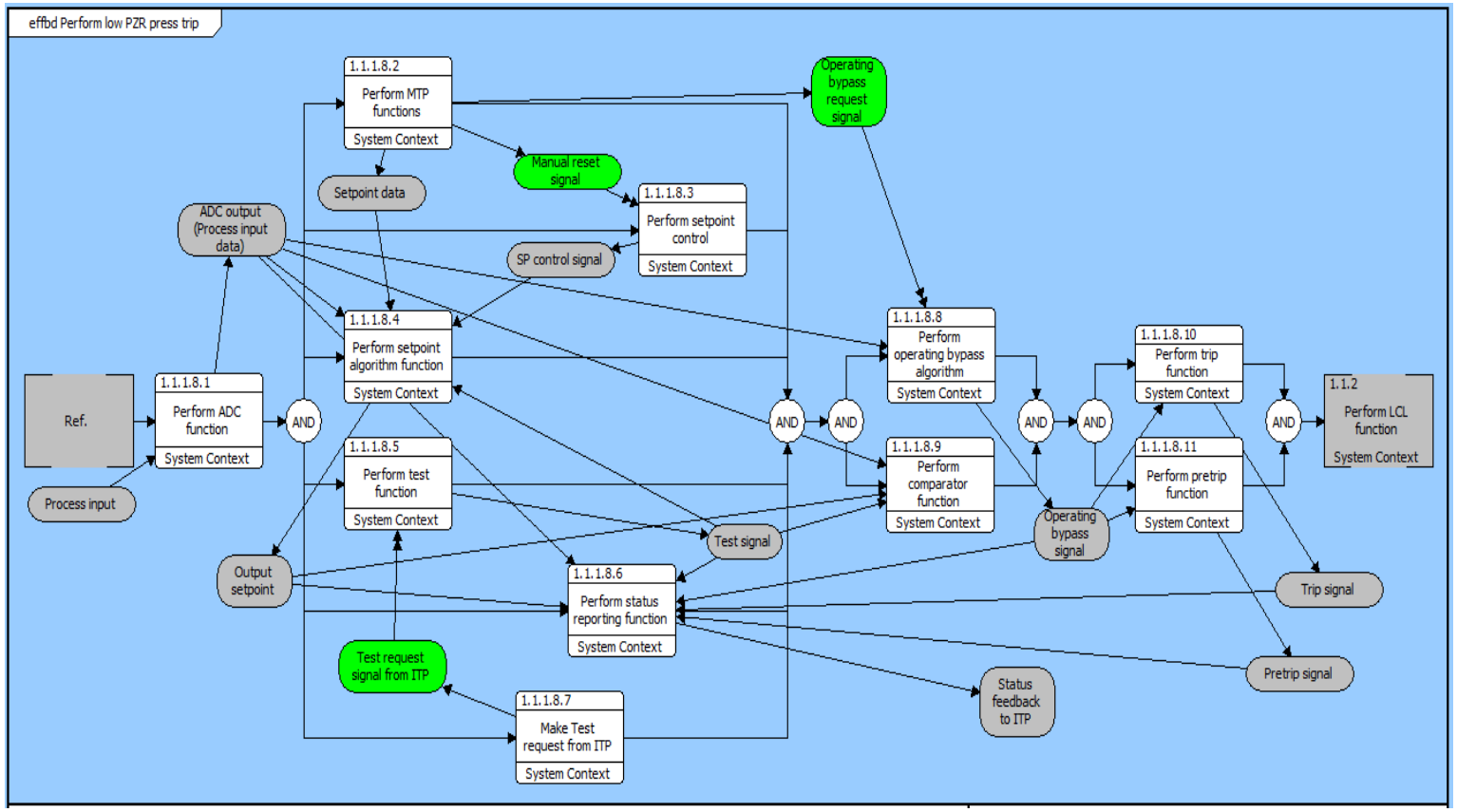


Bistable with variable manual reset setpoint - Trip on decreasing process (LPPT algorithm configurations)

METHODOLOGY

- ***EFFBD Model***
  - ❖ ***Functional flow verification of the BP logic block diagram***

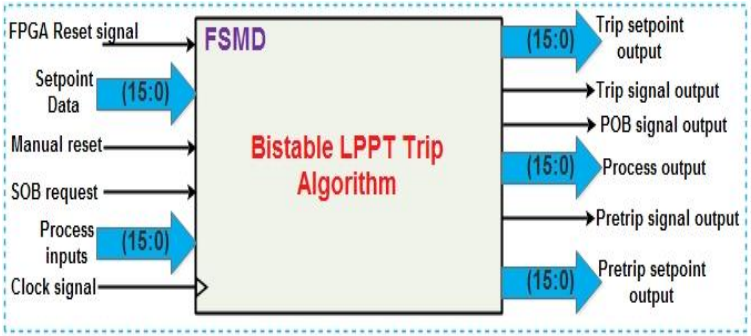
- Vitech's CORE® Model Based Systems engineering software tool is used to developed EFFBD



EFFBD (enhanced functional flow block diagram) model for LPPT.

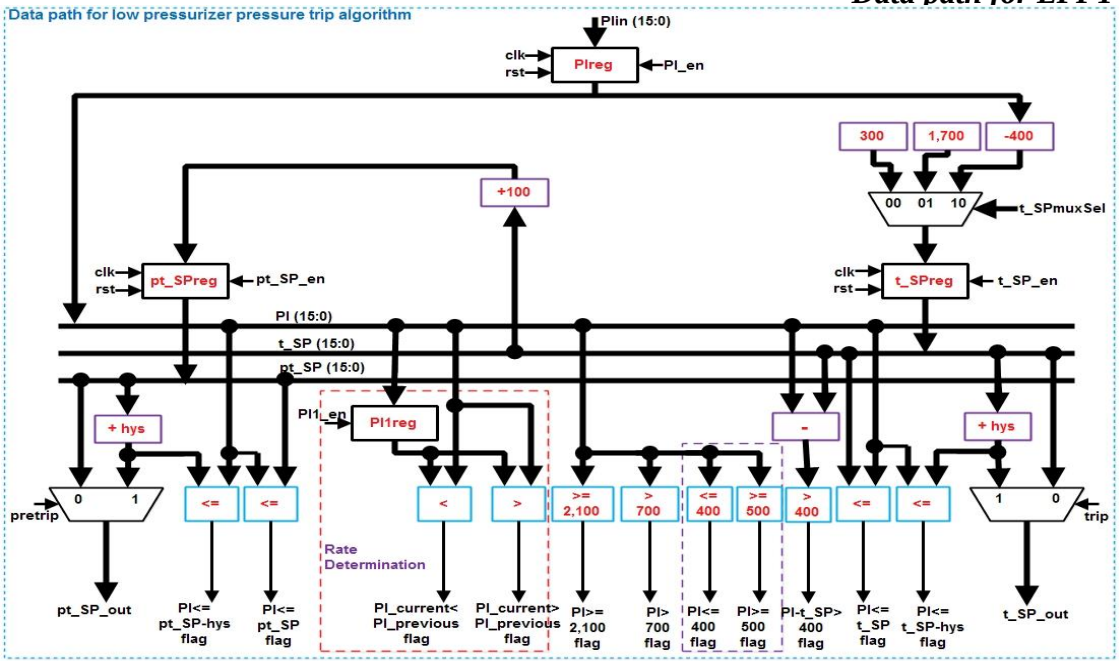
METHODOLOGY

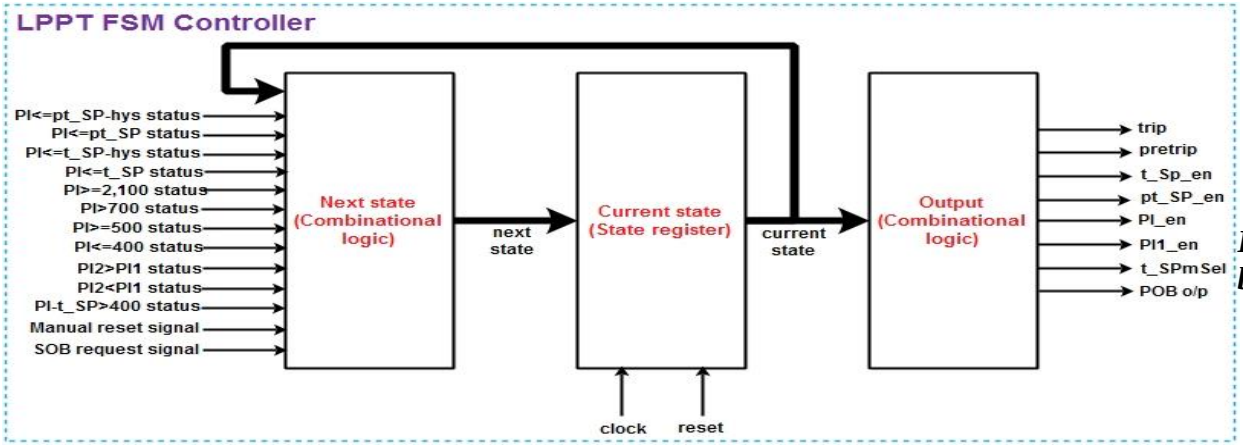
- *FSMD Model*
  - ❖ *LPPT Algorithm Design*



Interface Definition of FSMD for LPPT Algorithm

Data path for LPPT



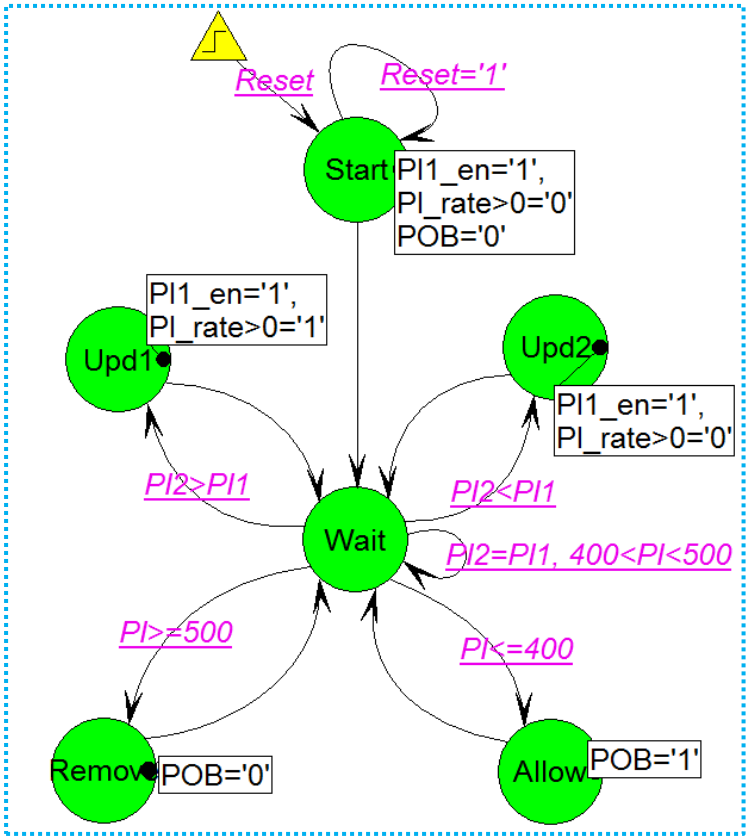


FSM controller block diagram

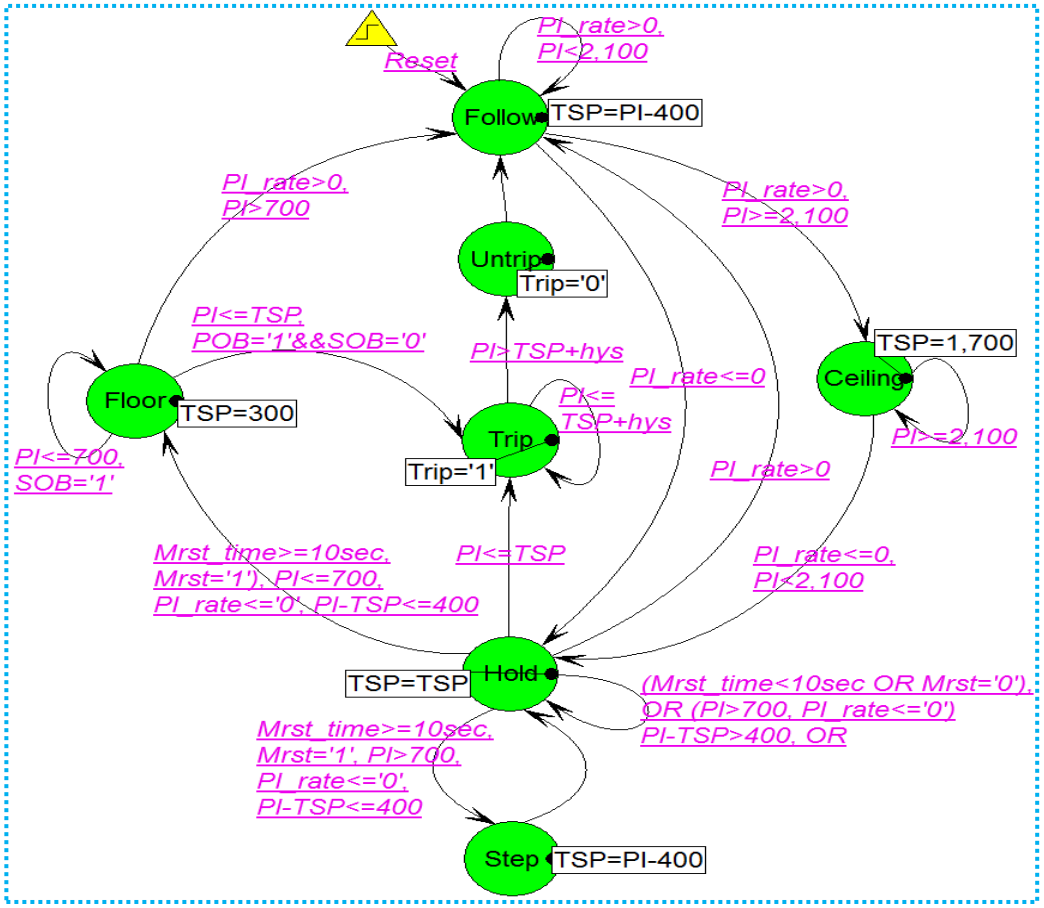
METHODOLOGY

- ***FSMD Model***
  - ❖ ***LPPT Algorithm Design***

LPPT State transition diagrams



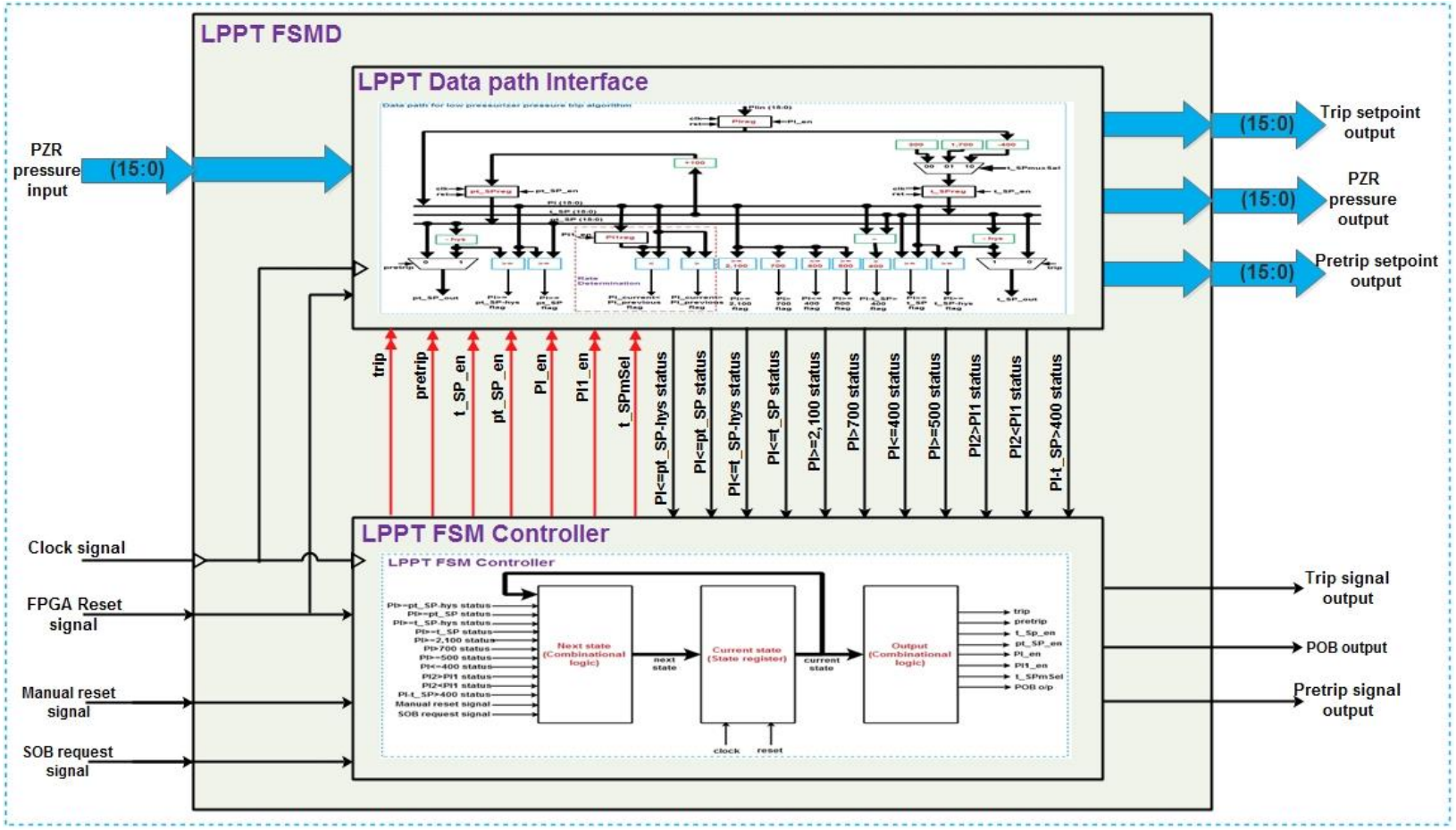
LPPT rate and Permission of operating bypass state transition diagram



LPPT trip setpoint calculation state transition diagram

METHODOLOGY

- ***FSMD Model***
  - ❖ ***LPPT algorithm design***

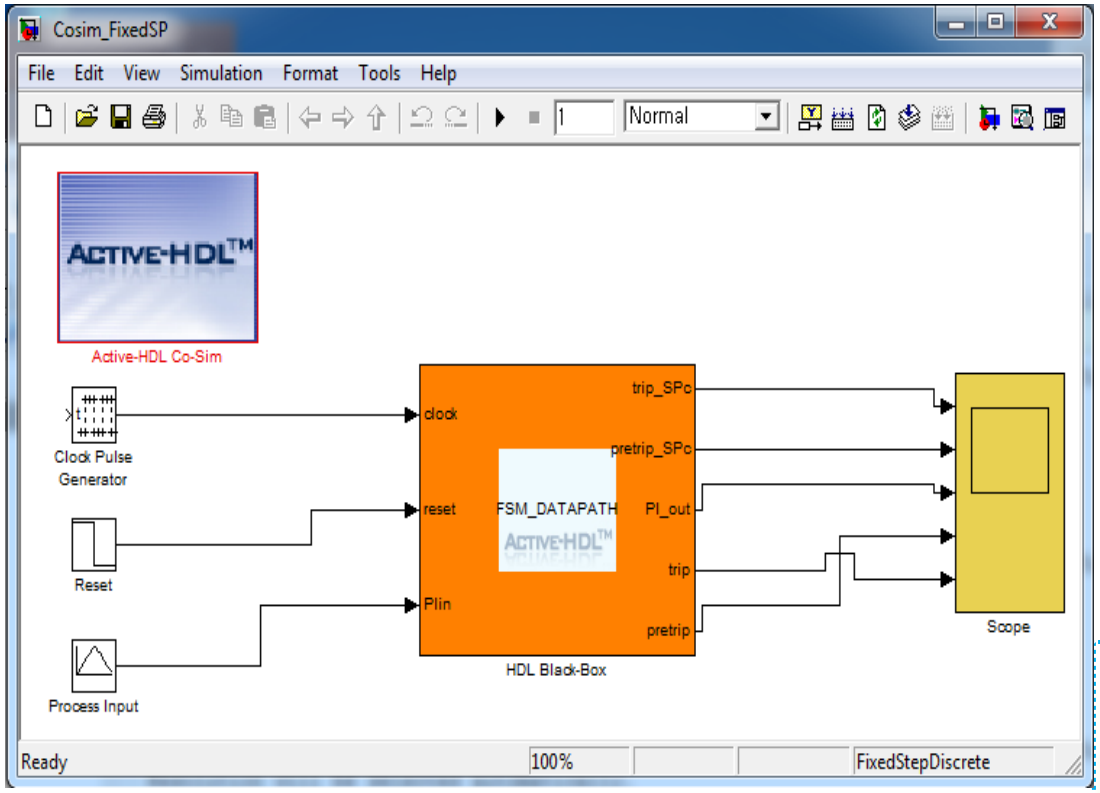


FSMD final design for LPPT configuration

METHODOLOGY

- *VHDL coding, and Design Verification and Validation*

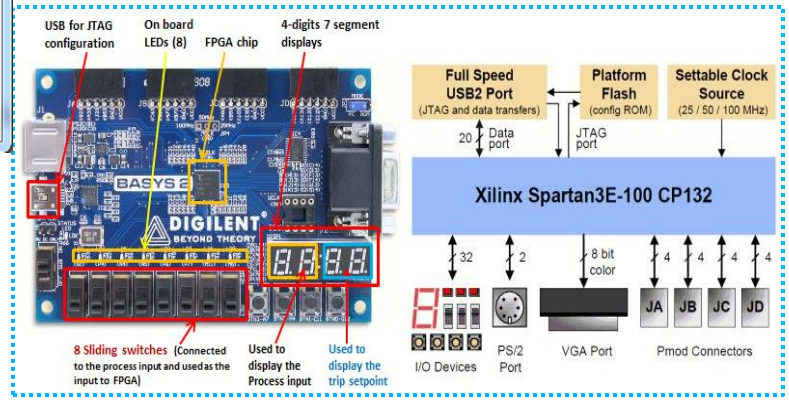
Simulink co-simulation model for fixed setpoint algorithm



Test bench Code using VHDL

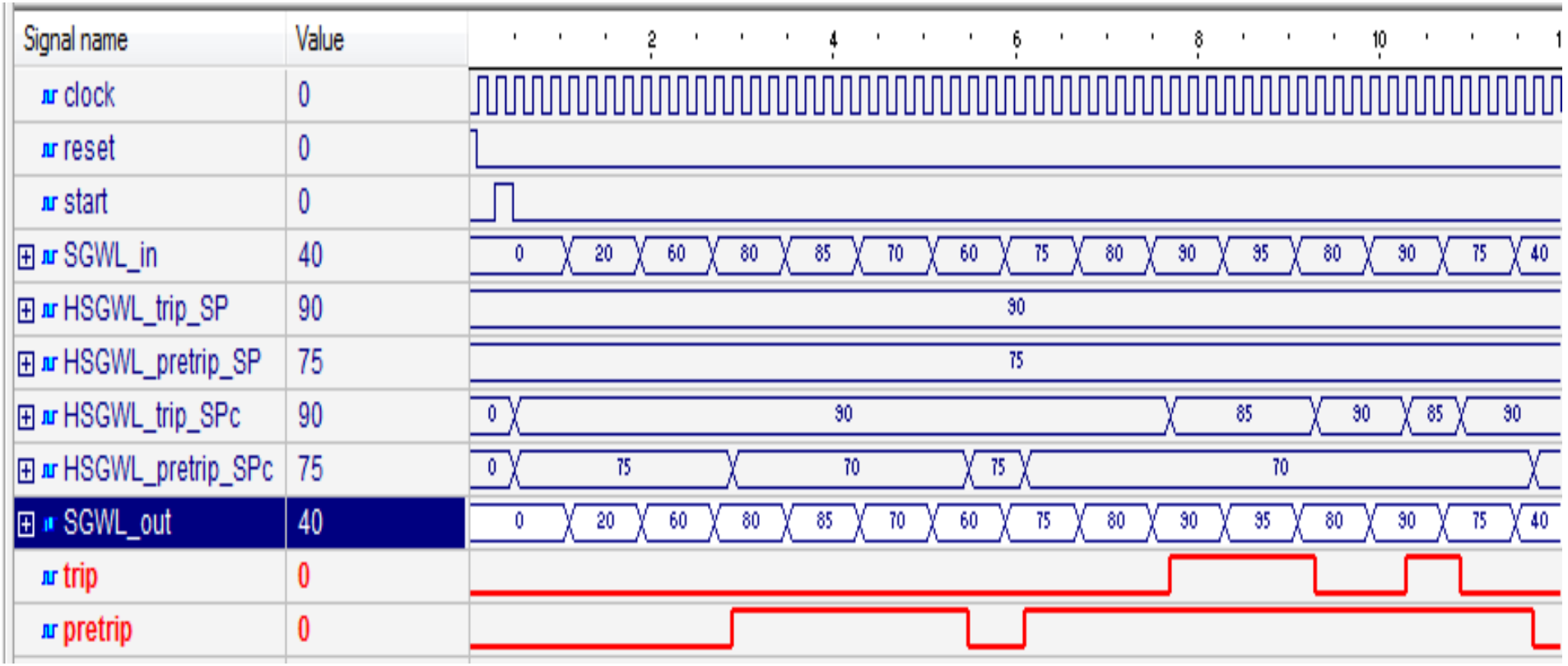
```
architecture OK_TB of OK_TB is
begin

    process
    begin
        wait for (period-(period*duty_cycle)
        reset <= '0';
        wait for period;
        RX_POWER_in <= "0000000000000000";
        wait for period;
        wait for (onerun+setup+tco);
        RX_POWER_in <= "0000000000001010";
        wait for period;
        wait for (onerun+setup+tco);
        RX_POWER_in <= "0000000000001111";
        wait for period;
        wait for (onerun+setup+tco);
        RX_POWER_in <= "0000000000011110";
        wait for period;
        wait for (onerun+setup+tco);
```



RESULTS

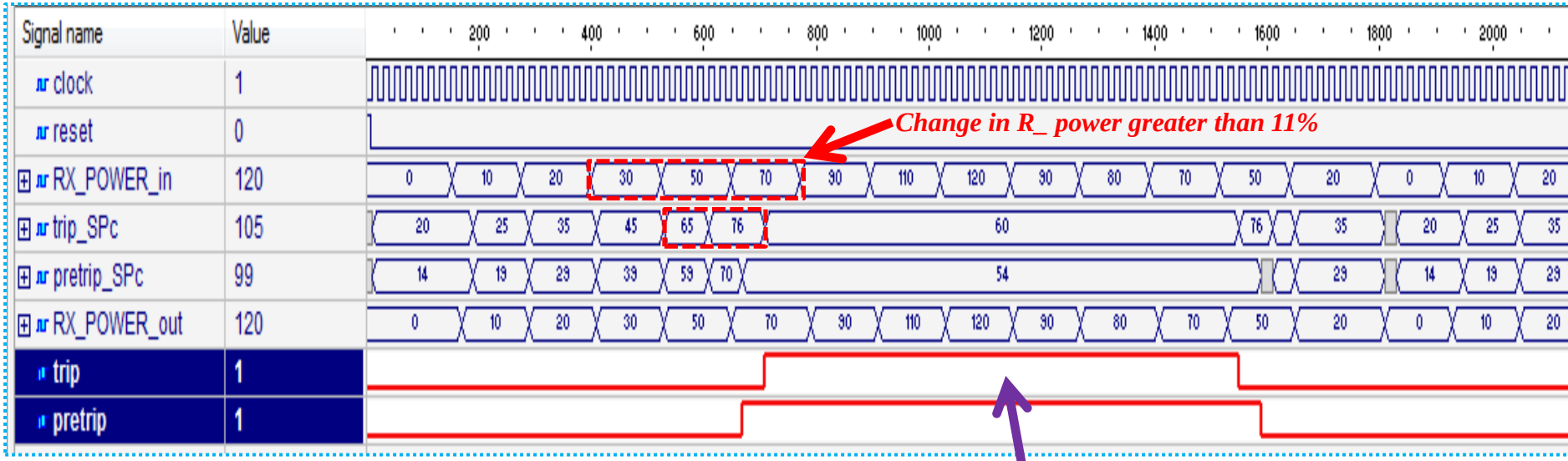
- ***Fixed Setpoint Simulation Result: High SGWL trip***



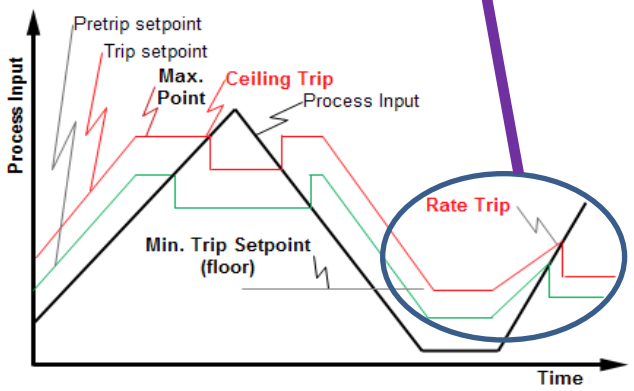
Fixed setpoint, steam generator water level trip simulation result from Active HDL simulator

RESULTS

- *VOPT Simulation Result: rate trip*

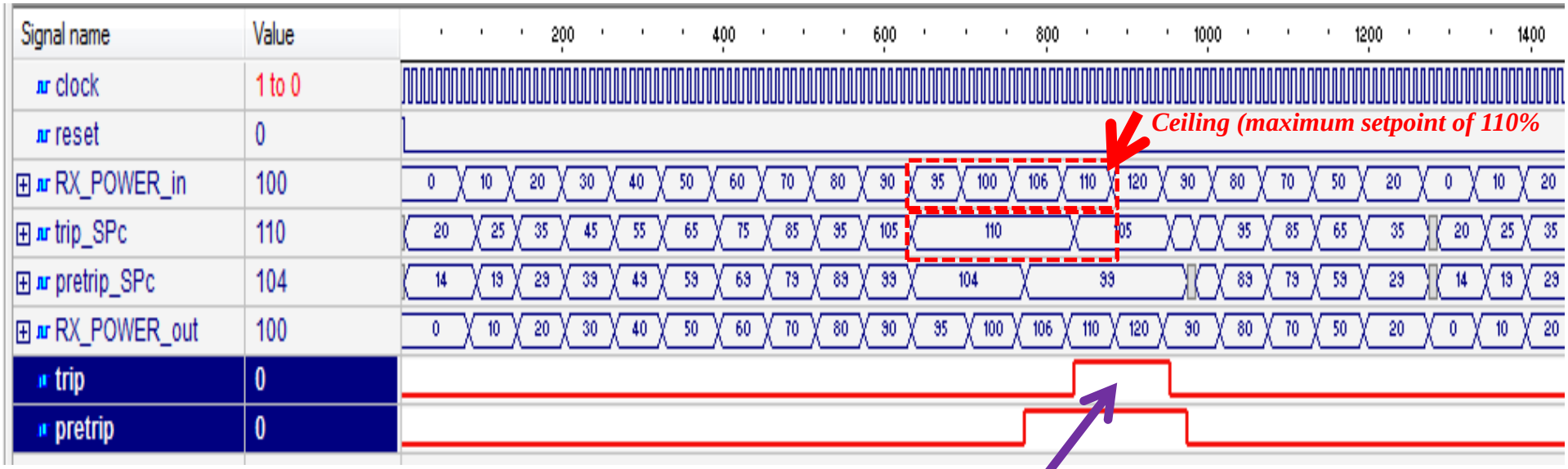


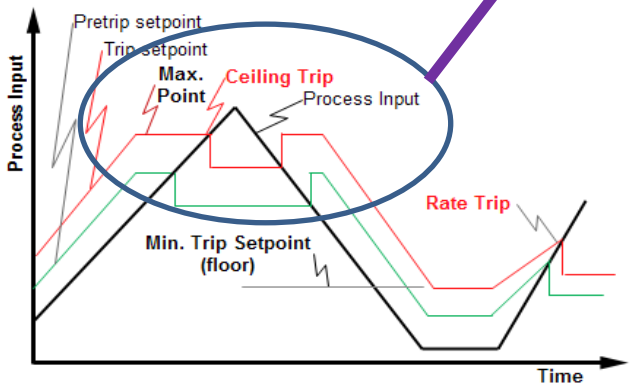
VOPT rate trip simulation result



RESULTS

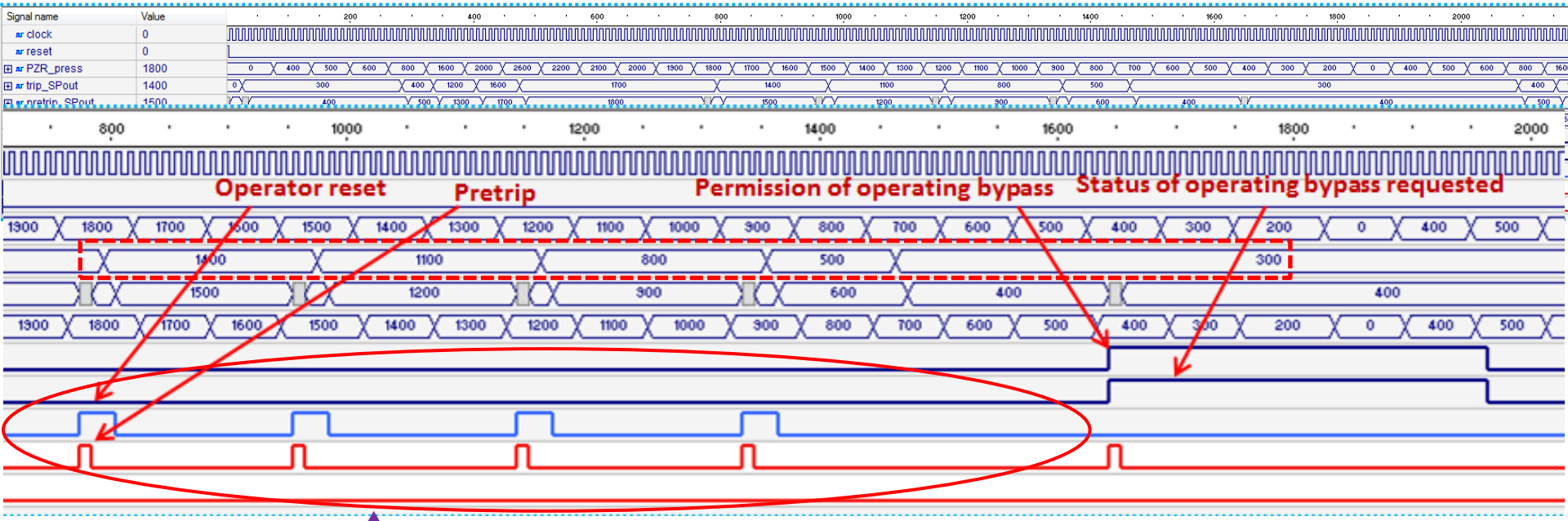
- *VOPT Simulation Result: Ceiling trip*

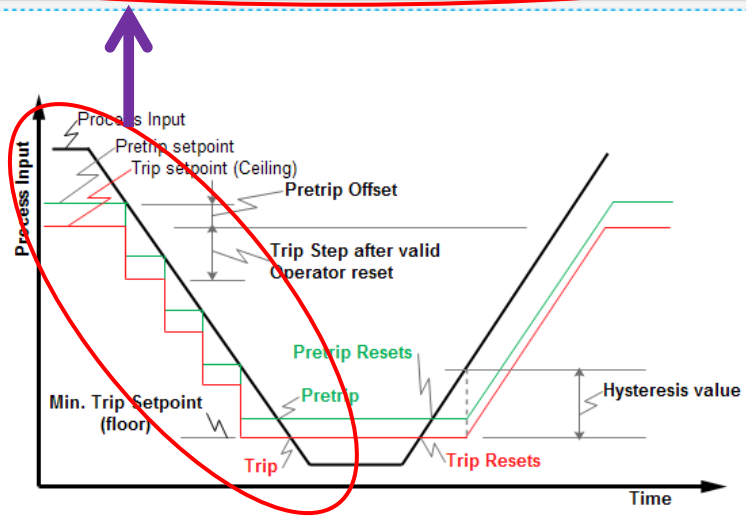




RESULTS

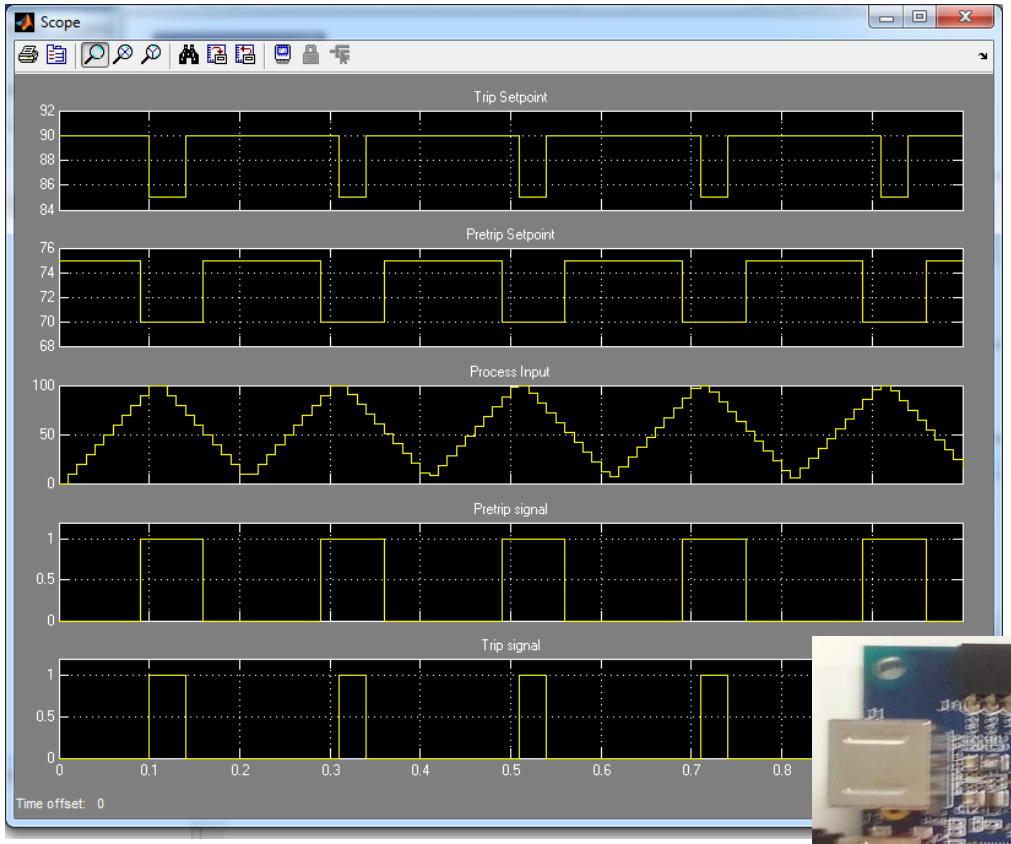
- *LPPT Simulation Result*

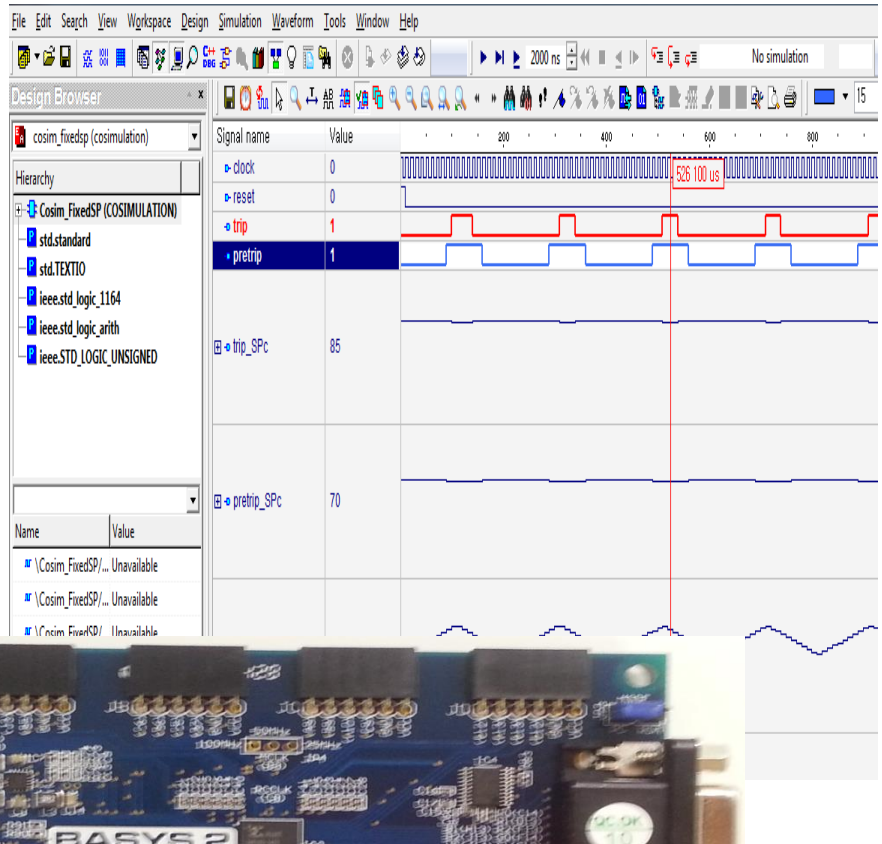


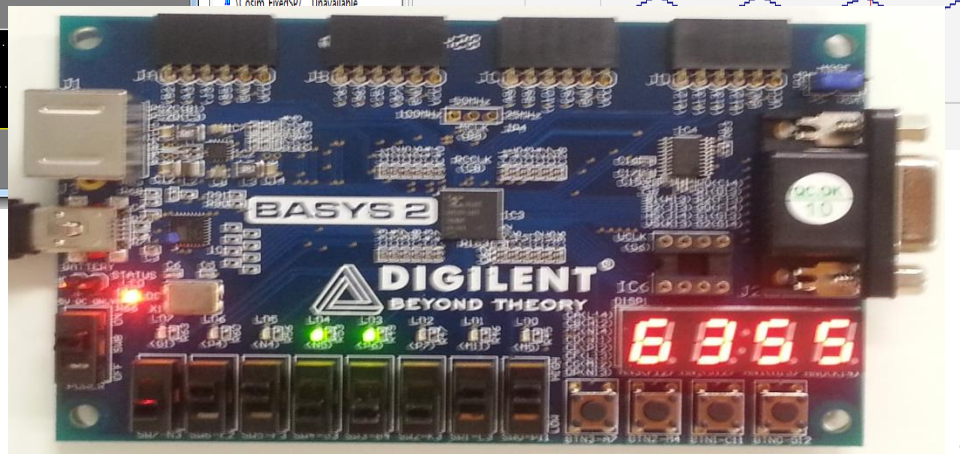


RESULTS

- ***Simulink Co-simulation Result for fixed setpoint***







On-board testing

CONCLUSION

- The PPS trip logic functions are designed, modeled, developed, verified, and validated in this work.
- The VHDL code is developed for each algorithm and the developed VHDL codes are verified and tested using Active-HDL tool.
- To further enhanced the design verification, an HDL Co-Simulation with MATLAB/SIMULINK is performed. It provides additional verification method for HDL design.
- To validate the design, the FPGA device is configured and tested. It operates without using the operating system or application software.
- Therefore, it can be concluded that, using the model-based approaches demonstrated in this work, together with co-simulation can enhanced the design verification as well as provides easy and quick HDL design verification.

Thank you

for

your attention