Design improvement of FPGA and CPU based digital circuit cards to solve timing issues

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1. Introduction

The digital circuit cards installed at NPPs (Nuclear Power Plant) are mostly composed of a CPU (Central Processing Unit) and a PLD (Programmable Logic Device; these include a FPGA (Field Programmable Gate Array) and a CPLD (Complex Programmable Logic Device)). This type of structure is typical and is maintained using digital circuit cards.

There are no big problems with this device as a structure. However, the data integrity problem is sometimes found cause a delay of the signal when the digital speed increases.

In particular, signal delay causes a lot of problems when various IC (Integrated Circuit) and several circuit cards are connected to the BUS of the backplane in the BUS design.

This paper suggests a structure to improve the BUS signal timing problems in a circuit card consisting of CPU and FPGA.

2. Digital Circuit Card

2.1 Structure of circuit card

In general, a digital circuit card is composed of a CPU, FPGA, Memory (RAM (Random Access Memory), ROM (Read Only Memory), FLASH, etc.) and various input/output terminals.

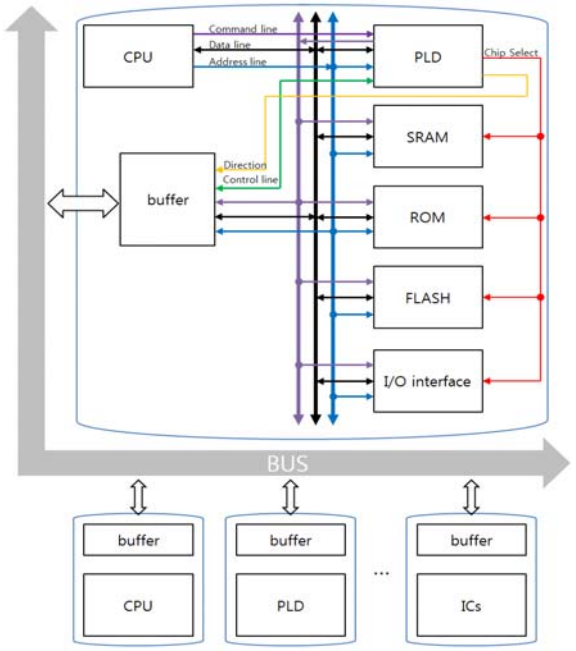

Figure 1 Signal block diagram of BUS and circuit card

Figure **1** shows the relation among the address, data, and control signals connected to the BUS.

All address signals are made by the CPU and transmitted to the various ICs, memories, and other circuit cards.

2.2 Data flow

The data perform read and write function via control signals of BUS. The BUS can be divided into two groups, synchronous and asynchronous, according to the synchronization of the clock. Figure **2** and Figure **3** show the read and write cycle [1].

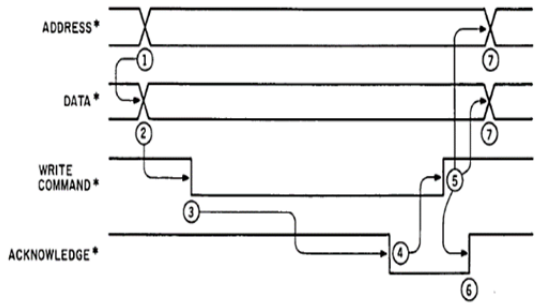

Figure 2 Write timing diagram

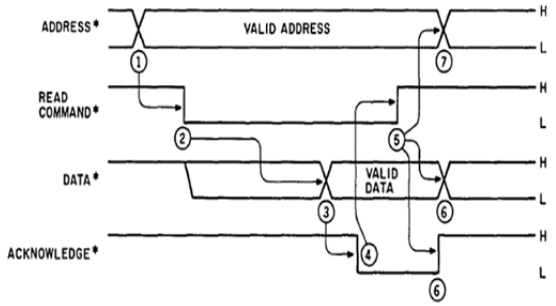

Figure 3 Read timing diagram

In order to guarantee the data integrity, the stability of the voltage level and the timing of the signal should be maintained.

3. Circuit Configuration and Signal Delay

3.1 How structure affects signal delay

If the signal source is generated at only one place, the signal delay time is constant. Of course, the delay time can be slightly different according to the wire length in the circuit card.

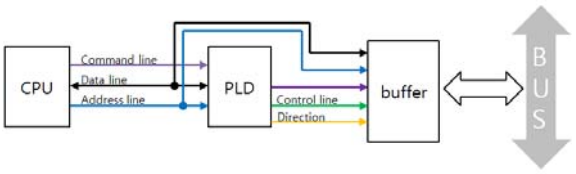

Figure 4 Signal path block diagram

As shown in Figure **4**, if the control line signals, direction signal, and chip select signal are made after PLD operation, final destination will receive control and BUS signals with different timings from the address and data.

3.2 Signal margin

As can be seen in Figure **5**, to maintain data integrity, the CPU generates command, address, and data line signals at required intervals.

However, the PLD existing between the CPU and the buffer performs decoding of the address and command. So, the PLD has 7ns of pin-to-pin delay and 10~20ns of operation delay [2].

In other words, the signal passing through the PLD and the signal directory passing through the buffer have delays of about 20~30ns [2].

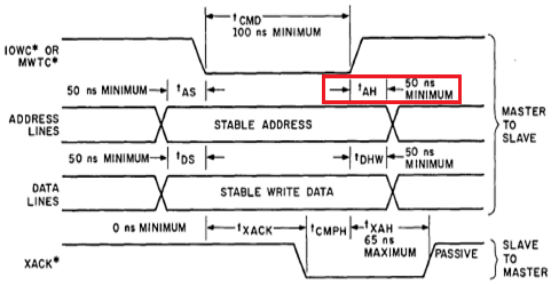

Figure 5 Signal timing generated and required in CPU

Address hold time (t_{AH}) is required to have a 50ns margin, as can be seen in Figure **5** [3], but it appears to have a time of 20~30ns except for the delay in real measurement, such as is shown in Figure **6**.

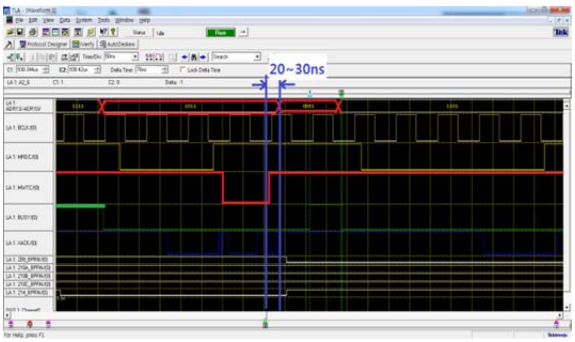

Figure 6 Real measured signals showing that delay occurred

3.3 Signal overlap

An ambiguity of signal is incurred by an overlap between the BUS control lines and the clock edge, as is shown in Figure **7**.

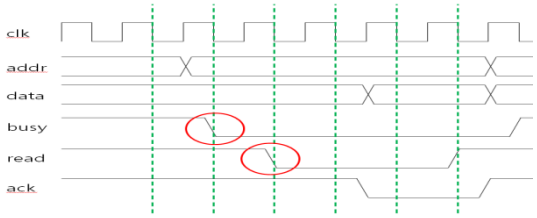

Figure 7 Overlap between clock and command due to signal delay

4. Suggested Design Improvement to Prevent Timing Errors

In signal processing, in order to prevent errors caused by signal delay, it is required to integrate all signal processing flow in a PLD.

4.1 Structure considering signal delay

The structure should be that shown in Figure 8 in order that address, data, and command lines generated by the CPU have same delay time.

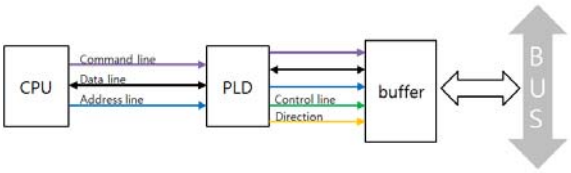

Figure 8 Signal path block diagram considering delay

If PLD as the BUS controller transfers and receives all data, it will make the data of the BUS flow smoothly.

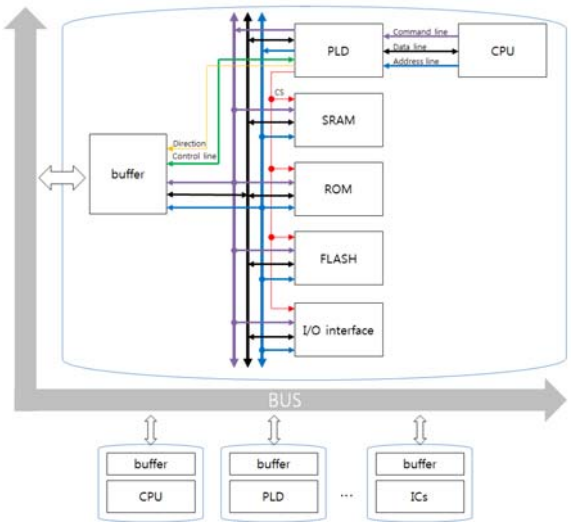

Figure 9 Relationship diagram of proposed BUS and circuit card signals

Figure 9 shows the structure of the rack design. In nuclear applications, even when both the BUS master and the slave circuits are located on the same control circuit card, the most ideal model is one in which the BUS master appears as a BUS slave on the backplane or on an extra circuit card for all other circuit cards.

4.2 Cycle effect of proposed structure

Although all input and output signals can have a default delay of a PLD, the delay does not have significant effects on the data flow of the BUS.

The performance of the BUS, of course, can decrease slightly.

One (1) cycle has a maximum of one (1) clock delay at the beginning and at the end of the cycle. If the clock is 10MHz, the delay is about 200ns.

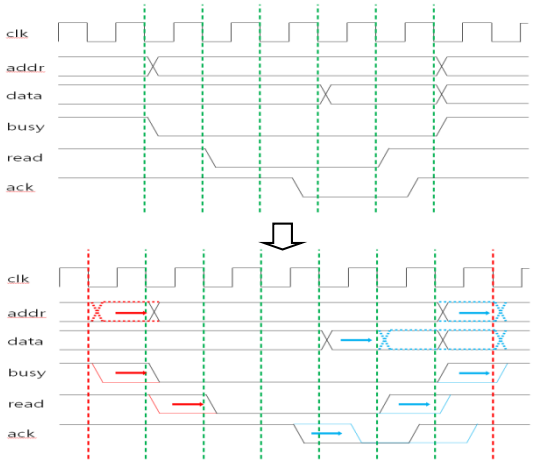

Figure 10 Cycle time increment due to PLD operation

As can be seen in Figure 10, if one (1) cycle (standard busy signal) of a read and a write is normally 400~500ns (4~5 clock), it will increase by about 600~700ns for a maximum of two (2) clocks.

But, a 200ns increase in one (1) cycle does not significantly affect the data flow. Table I is a one (1) cycle comparison table of one (1) cycle between the existing structure and the proposed one.

Table I: Comparison of existing and proposed cycle times

Items	Existing cycle time	Proposed cycle time
Base clock	10MHz	10MHz
Read cycle	5 clock, 500ns	7 clock, 700ns (max.)
Write cycle	4 clock, 400ns	6 clock, 600ns (max.)
Gap between address and command	Appx. 30ns	Appx. 0ns

5. Conclusions

Nowadays, as the structure of circuit cards has become complex and mass data at high speed is communicated through the BUS, data integrity is the most important issue.

The conventional design does not consider delay and the synchronicity of signal and this causes many problems in data processing.

In order to solve these problems, it is important to isolate the BUS controller from the CPU and maintain constancy of the signal delay by using a PLD.

In future work, it is necessary to study how to maintain the independence of the data flow control of the BUS by designing a BUS controller as a separate card.

REFERENCES

[1] James B. Johnson, Steve Kassel, “The Multibus design guidebook”, McGraw-Hill Book Company, p44-45, 1984.
[2] Datasheet, “XC95216 In-System Programmable CPLD”, Xilinx INC., p1-4, 2013.
[3] IEEE 796, “Standard Microcomputer System Bus”, p30, 1983.