Development of Final Running Test System for Digital Systems

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1. Introduction

The digital control systems consist of various types of control hardware, control & MMI software, and the networks. In general, the control systems perform the control functions by exchanging information via the communication networks between several control cabinets.

In nuclear industry, the newly designed systems to upgrade are qualified to meet IEEE standards and the regulatory guidelines for their functions, performance and reliability requirements. Failure Mode & Effect Analysis, Fault Tree Analysis, and Hazard Analysis have been used to improve the reliability of the control system. To ensure the completeness of the software, the verification and validation processes are carried out during the development process.

In spite of the many efforts depending on the analysis and procedures, there are limitations to improve the reliability [1]. The lessons learned from the currently installed system failures show the incompleteness of the final integration test [2]. The current point-to-point and logic-to-logic separate test procedures manually performed by the engineers can cause some procedures missed and have effects on the critical functions.

As an end user of the digital systems, the various attempts to improve the reliability of the current process have been considered. One of them is an improvement of the test method.

In this paper, we propose a Final Running Test method and equipment necessary to ensure the digital system integrity.

2. Conventional Test Method

Figure 1 shows the typical digital system upgrade process. The supplier designs, fabricates, and tests to meet the system requirements. All processes are done under the quality assurance program. To ensure the software integrity, the verification and validation planning and procedures are performed. After development is completed, Factory Acceptance Test, Site Acceptance Test, and Startup Test are carried out before system operation.

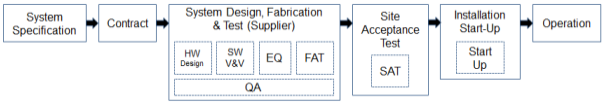

Fig. 1. The typical upgrade process of the digital system

FAT or SAT is a process of confirming the limited functionality and performance during a relatively short time. Because SAT is the final validation test performed prior to installation, it should cover the wide range of operating conditions if possible.

So, the computer-controlled test device that can effectively perform a wide range of test cases is needed.

Figure 2 shows an improved SAT including the automatic computerized Final Running Test capability.

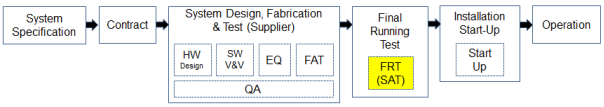

Fig. 2. SAT with Final Running Test

FRT covers a variety of the test cases systematically more than the conventional approach and provides the real time test evaluation results using the test patterns.

3. Design of Final Running Test System

3.1 Overview of FRT System

Figure 3 shows the overview of FRT system. FRT system consists of Test Operating System and Control & Monitoring System. TOS provides various test scenarios to the test systems, and controls, monitors the input and output signals. The process simulator in the TOS provides dynamic responses of the specific plant process needed to a test system. The test scenarios can be made, edited, and modified in the test operating computer. The real-time check computer evaluates the test results in real time.

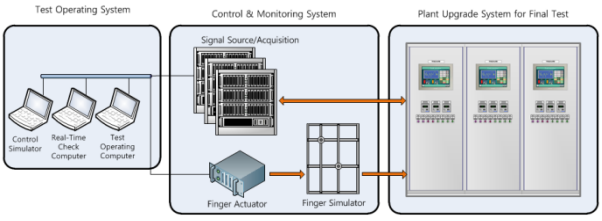

Fig. 3. The overview of FRT system

The signal sources and acquisition modules in the Control & Monitoring System provide a number of test signals suitable for the test system and obtain the responding output signals. The finger simulator simulates the finger motion to operate the touch screen monitor.

The test systems for plant upgrade can be any type of digital systems including NSSS Control Systems, Plant Monitoring Systems, and Plant Protection Systems. The plant process dynamics may be represented by the

combination of a few of the representative formula listed in Table 1.

Table 1 : Process Dynamics Formulas

No	Description	Formulas
1	Dead Time with Gain	$K_p e^{-\theta s}$
2	First-Order with Dead Time and Gain	$\frac{K_p e^{-\theta s}}{1+\tau s}$
3	Second-Order with Dead Time and Gain	$\frac{K_p e^{-\theta s}}{(1+\tau_1 s)(1+\tau_2 s)}$
4	Second-Order Over-Damped with Dead Time (Imaginary Roots) and Gain	$\frac{K_p e^{-\theta s}}{(1+P_1 s)(1+P_2 s^2)}$
5	Integrator with Dead Time	$\frac{e^{-\theta s}}{\tau s}$
6	Integrator with First-Order and Dead Time	$\frac{e^{-\theta s}}{\tau_1 s+\tau_2 s^2}$
7	Inverse Response Process or Shrink-Swell ; Integrator with First-Order, Lead Time, and Dead Time	$\frac{(1+\tau_1 s)e^{-\theta s}}{\tau_2 s+\tau_3 s^2}$
8	Double Integrator with Dead Time	$\frac{e^{-\theta s}}{\tau s^2}$

3.2 Test Evaluation Method using Control Patterns

Fig. 4 shows the example of the response control patterns composed of the input/output signals, operator actuation patterns. The reference signal patterns are acquired from the manually tested control system. The measured signals can be acquired in real time for each single test cycle.

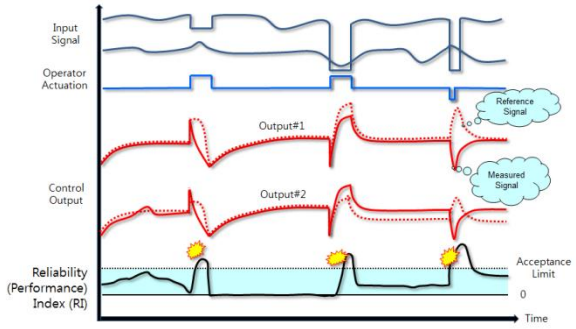

Fig. 4 Control Patterns Examples

The acceptance limit of FRT can vary depending on the system criticality. The RI(Reliability Index) value is calculated and evaluated in real time to show the system integrity during the final running period. The RI function can be made with the complex relationships between the measured variables and statistically processed results.

When RI values go higher than the acceptance limit, the system under the test assessed as an unreliable one or unsatisfactory one in some cases.

3.3 Test System for Demonstration

To evaluate the feasibility of the test method and the FRT system, the test systems will be designed and purchased this year.

The selection criteria of the demonstration systems are the recently installed system and the latest proven digital system, and reasonable price for test setup. The demonstration systems selected are Ovation DCS, OPERA DCS, HFC PCS, and ControlLogix PLC. The selected systems will have some plant system functionalities partially such as NSSS Control System and ESF-Component Control System.

3. Conclusions

The design processes of the digital systems are met in accordance with the international standards and regulatory guideliness. The lessons learned from the failures of the running digital systems showed the limitations of the current verification and validation efforts. The various improvements and attempts have been considered including the expert review processes and the completeness of the test.

In this paper, the Final Running Test Method evaluating the completeness of the digital system using the control patterns and the Test System Architecture are proposed. The feasibility and the effectiveness of this proposal will be performed in this year.

REFERENCES

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