Verification of FPGA-Signal using the test board which is applied to Safety-related controller

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1. Introduction

This article aims to provide the verification method for BGA-type FPGA of Programmable Logic Controller (PLC) developed as Safety Class. The logic of FPGA in the control device with Safety Class is the circuit to control overall logic of PLC.

Saftety-related PLC must meet the international standard specifications. With this reason, we use V & V according to an international standard in order to secure high reliability and safety. By using this, we are supposed to proceed to a variety of verification courses for extra reliability and safety analysis.

In order to have efficient verification of test results, we propose the test using the newly changed BGA socket which can resolve the problems of the conventional socket on this paper.

2. Introduce method of verification for Safety-class

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The Verification of processes is divided into verification of Hardware and firmware. That processes are carried out in the unit testing and integration testing.

Firmware test must be verified in accordance with the V-Model life cycle of IEEE 1074 and the Life Cycle of the Software is shown on the picture below.

SW CT, IT, ST test among the Software Life cycles determines the validity of digital logic circuit and also checks whether the signal of the designed circuit is properly working.

Therefore, Module-based PLC requires the test for all the modules. which can provide convenience for the test by taking advantage of the socket.

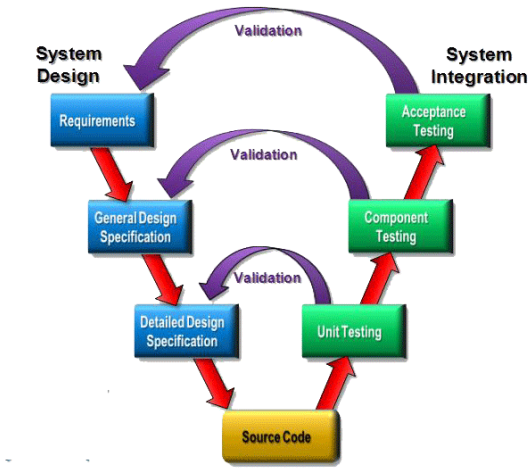

Fig.1. IEEE 1074 Software Life Cycle(V-Model)

Among the following processes, the direct verification with FPGA, which is required for the last verification process, is the process of live data verification, and it should measure the signals related to the roles of blocks. Therefore, a complex wiring process is required and it must go through a process to identify and verify multiple data.

3. Problem of method at former socket

(BGA) type IC is arrayed by the terminals of IC, which are balls, on the whole surface of the IC plate, minimizing the size and thickness of IC innovatively. Because Pin is not exposed in BGA Type IC, its data acquisition is challenging. Accessing each Pin data of the device to the circuit line directly, it analyzed the data by analyzer. Due to this, it had the problem on the data reliability, moreover, it took a long time to detect the signal. Also, because of the multiple disconnections, there were many cases to get damages on IC directly while acquiring the data.

To simplify this complicated test, we can prevent it from being damaged by minimizing the contact pressure applied to the BGA. During the last seminar, we have proposed the existing socket which could improve the test reliability by facilitating physical and electrical connection with BGA.

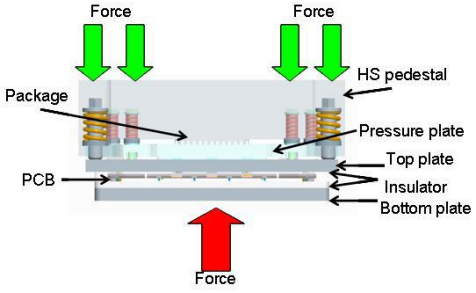

Fig 2. Contact pin of previously socket

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However, we applied force to the existing processor to have the signal accuracy and to minimize the contact surface, which accordingly caused bending of the PCB due to the heavy weight of the socket.

4. Compare of former socket

Previously we had to press the FPGA to secure FPGA's signal-accuracy, measuring the signal by connecting FPGA pins and the socket around FPGA.

Using the newly enhanced method, we can measure the signal through the signal measurement device by setting the jumpers on the PCB and connecting it to the other board in order to measure the FPGA signal

This new approach does not only reduce the weight of the PCB but also decreases signal interference from the measurement equipment, which allows us to easily and conveniently check the data and its operation.

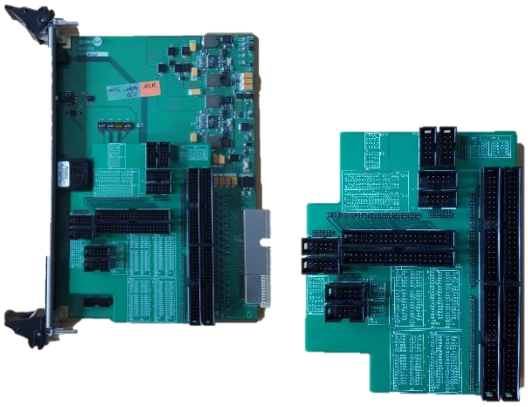

Fig 3. Test board

The right side picture is testing boarding and left side picture is equipped with a jumper on the board

5.0 Signal analysis of test

We produced the pilot product and installed it to the live module. Then, we tested it whether all the signals were properly operated.

The below picture is the module installed with BGA using by testing board of the produced module.

Fig .4. verification of using test board

6. Conclusion

The proposed test method is simple, the effect of cost reductions by batch process.

In addition, it is advantageous to measure the signal from the Hi-speed-IC due to its short length of the pins and it was plated with the copper around it. Further, it also to prevent abrasion on the IC ball because it has no direct contact with the PCB.

Therefore, it can be actually applied is to the BGA package test and we can easily verify logic as well as easily checking the operation of the designed data

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