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Radiation Hardening and Verification Procedure for Compact Flip-Flop Design

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1. Introduction

For radiation-related applications applying electronic devices in nuclear, space, medicine, and scientific experiment, single event transients (SETs) and single event upsets (SEUs) are become primary concern since they can cause malfunctions in a system by affecting the signal transition and flipping digital bits.

As shown in Fig. 1, the effect of SETs is the contamination of data with a range of amplitudes and durations in a logic stage between registers mainly composed of flip-flops. The D flip-flop as a register is generally used in digital circuits that require data stability and high speed.

For many years, radiation-hardened-by-design (RHBD) circuits have been gradually developed from traditional circuit architectures. One of common methods is to exploit redundancy in an important circuit block to preserve the correct signal. This technique uses a voting process to have a correct output when other duplicated systems fail due to a single event effect (SEE) including SET and SEU. For instance, B. Olson applied the redundancy technique, formally referred the triple modular redundancy (TMR) [2]. Additionally, a dual-path hardening technique implemented on a multiplying digital-to-analog converter circuit (MDAC) and a comparator circuit introduces significant radiation hardening. Other researchers use various error detection and correction (EDAC) algorithms including redundant bits in the storage circuits to detect and correct errors at the system level [3]. These methods have been successfully utilized in applications requiring radiation hardening; however, all of them lead to various penalties in speed, area and resolution by adding components such as TMR, voting circuits, and extra bits for EDAC methods. TMR usually requires a three times expansion in area and power consumption for redundancy circuits and EDAC inevitably needs more calculation time as well as redundancy data storages.

In order to mitigate this hardware and software burden, an error detection flip-flop was designed for clock-based digital circuits [4]. This technique allows a digital system to detect a delayed signal as an error induced from SET and recovery the error by reproducing the failed calculation.

2. D Flip-Flop Design

2.1. Conventional D flip-flop

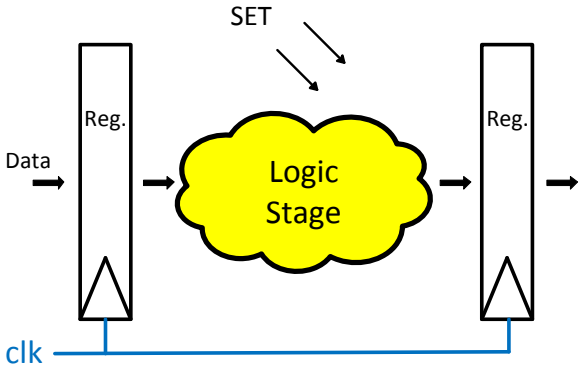

Fig. 1. A conventional logic stage with registers in a digital circuit [1].

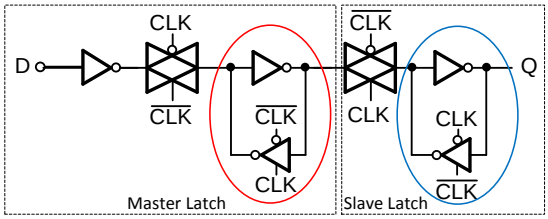

Fig. 2. A conventional D Flip-Flop design [1].

Briefly introducing the conventional D Flip-Flop (DFF) of Fig. 2, when the clock goes down, the master latch is ready to store calculated data from the previous logic stage (red circle not activated) while the slave latch keeps propagating stored data for the next stage in the storage system (blue circle). At the rising edge of the clock, the data from the previous stage is ideally "locked" and stored in the master latch (red circle) during the clock high. With this mechanism in a clock based digital circuit, data in both "transition" and "storage" phases are literally exposed to radiation impact events.

2.2. Radiation Hardened D flip-flop

The radiation hardened DFF operates identically to a normal DFF when no SET violation occurs. While the clock goes down, the virtual rails (VVDD and VVSS) monitor any input signal (D) transitions, and DN is driven to be the inverted D. After the clock rises, one of the virtual rails turns floating since clocking transistors, M1 and M4, in Fig. 3 are turned off. However, either VVDD or VVSS still remains connected to DN depending on the state of D. As long as D remains in the same state as no radiation error events when the master stage closed, DN keeps equal to the connected virtual rail. If D changes while in the state due to SET at the

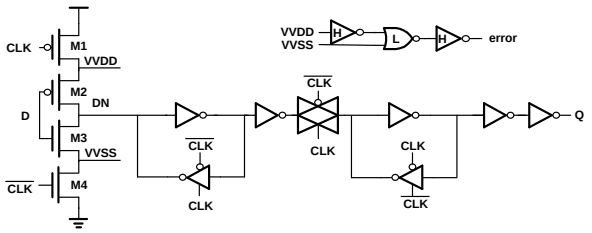

Fig. 3. Radiation hardened D Flip-Flop design [4].

previous stage, the floated virtual rail suddenly becomes connected to DN. Since that virtual rail originally has the opposite state as DN, this is (dis)charged the virtual rail by the feedback inverter of the master latch. For instance, assume that D is logically high (DN is low) while clock goes high. VVDD is then at a floating state with M2 off and VVSS is connected to DN, that is, low. If D suddenly changes low due to SEE (while clock is high), M3 will turn off while M2 turns on, changing VVDD high to ground through the feedback inverter and M2. Analogously, VVSS switches from low to high when input D transitions high after the clock rises. By monitoring these two virtual rails, an SET error signal can be generated.

3. Fabrication and Verification Procedure

In order to verify the radiation tolerant ability of semiconductor devices, the primary decision would be the process selection as described in Table I. Any integrated circuits have shown fairly different performances depending on what fabrication technology was chosen even though their functionalities in transistor level are identical. Therefore, target technologies should be carefully selected and followed by specifying circuit design. Circuits designed in different technologies should also have similar performance and functions in comparison to each other as a figure of metric.

The next verification step is a layout process. The performance of a designed circuit could be varied by how it was layouted. For the intensive analysis of radiation hardening ability, circuit designers should prudently decide the geometrics of a transistor such as width, length, fingering, and distance. These physical changes will lead to unexpected uncertainties on its radiation hardened capability.

Table I: Verification Procedure for RHBD Circuits

	Work	Subtask
1	Process Selection	- Different devices (BJT and CMOS) - Different fabrication processes (180 nm and 130 nm)
2	Layout	- Conventional vs. RHBD - Different sizing - Different placement
3	Fabrication	- Through manufacturers
4	Radiation Exposing Experiment	- ^{60}Co experimental facility at KAERI - Different dose and time

The last procedure after fabrication by semiconductor manufacturers is practical experiments at radiation exposure facilities. Korea Atomic Energy Research Institute (KAERI) operates a laboratory with high energy radioactive isotope, ^{60}Co in Jeongeup, Korea. The facility can provide various experiments requiring experimental environment changes by controlling radiation activity and radiated energy.

4. Future Work

The future direction on RHBD circuits would be integration with the digital DFF presented in this paper and analog front-end units such as OP-amp for charge-sensitive or shaping amplifier. Analog-to-digital converters (ADCs) are also major components necessarily imbedded in the most of sensor related electronics. Thus RHBD techniques are inevitably required to protect these circuits from SEE; specifically, SEUs for digital logics and SETs for analog signals. Since most ADCs consist of both analog and digital circuits in their architectures, SEE can cause significant malfunction in a system that composes radiation intolerant ADCs and/or DACs. Therefore, well-developed RHBD techniques on ADC design are mandatorily required for radiation-tolerant applications.

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