Implementation of KoHLT-EB DAQ System using compact RIO with EPICS

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1. Introduction

EPICS (Experimental Physics and Industrial Control System) is a collection of software tools collaboratively developed which can be integrated to provide a comprehensive and scalable control system. Currently there is an increase in use of such systems in large Physics experiments like KSTAR, ITER and DAIC (Daejeon Accelerator Ion Complex).

The Korean heat load test facility (KoHLT-EB) was installed at KAERI. This facility is utilized for a qualification test of the plasma facing component (PFC) for the ITER first wall and DEMO divertor, and the thermo-hydraulic experiments [1]. The existing data acquisition device was Agilent 34980A multifunction switch and measurement unit and controlled by Agilent VEE.

In the present paper, we report the EPICS based newly upgraded KoHLT-EB DAQ system which is the advanced data acquisition system using FPGA-based reconfigurable DAQ devices like compact RIO.

2. Data acquisition system of KoHLT-EB

An electron beam facility is now in operation to conduct the cyclic heat load experiments for the plasma facing components, as shown in Fig. 1.

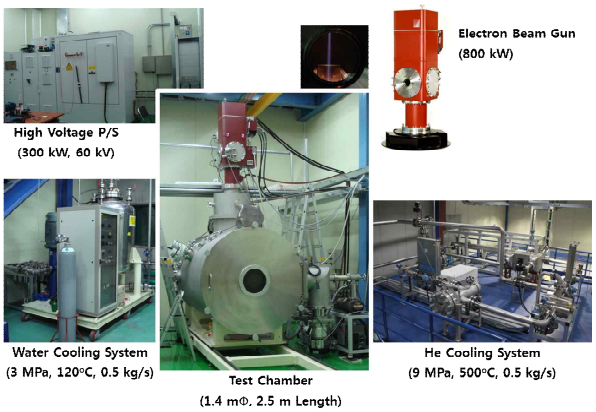

Fig. 1 High heat flex test facility

2.1 Agilent 34980A based DAQ system

The existing DAQ system was composed of Agilent 34980A and 34925A module, as shown in Fig. 2.

Agilent 34980A based DAQ system was able to measure up to 25 data set per second.

	Calorimeter	NBDLM
Mock-up T/C	5	20
Calorimetric heat flux T/C	2	2
Flow meter	1	1
Inlet pressure	1	1
Pressure drop	1	1
Total	10	25

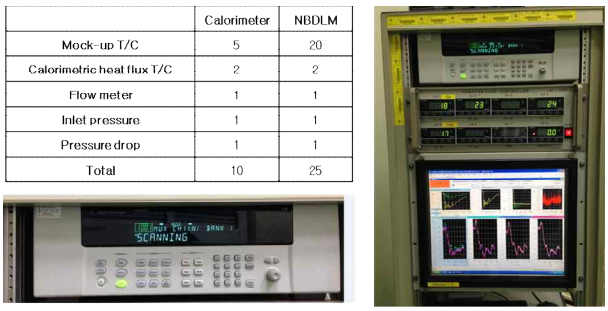

Fig. 2 Agilent 34980A based KoHLT-EB DAS

2.2 FPGA

Field Programmable Gate Arrays (FPGAs) are reprogrammable silicon chips. Using prebuilt logic blocks and programmable routing resources, FPGAs can be programmed to the desired application or functionality requirements.

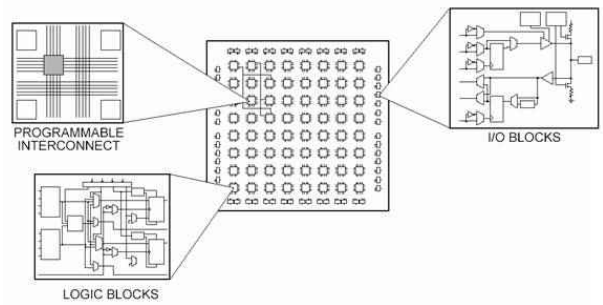

Fig. 3 Scheme of the elements of a FPGA

Fig. 3 shows the main elements which the FPGA is composed by.

2.3 NI compact RIO

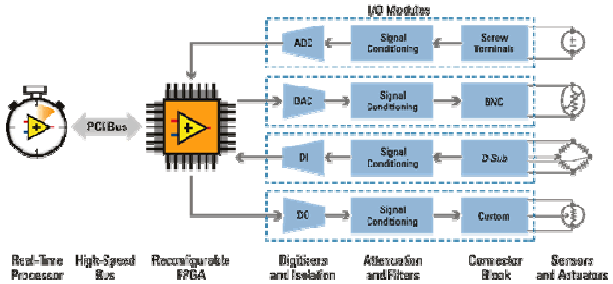

Fig. 4 NI RIO Architecture Diagram

The reconfigurable I/O (RIO) architecture combines the graphical programming environment with processor, a reconfigurable FPGA and I/O modules for measurement and/or acquisition, as shown in Fig. 4.

The reconfigurable FPGA is the core of the RIO hardware system architecture and it has each module connected directly to the FPGA rather than through a bus. Then there is almost no control latency for system response compared to other industrial controllers [2].

Compact RIO is a small, rugged RIO system for embedded and prototyping applications, Configurable with four- , eight-, and fourteen-slot backplanes. It contains two main components: a reconfigurable FPGA in a chassis, and the interchangeable industrial I/O modules. The Compact RIO system can be connected to a computer using a PCIe link. The embedded chassis contains the reconfigurable I/O FPGA chip directly connected to I/O modules that deliver diverse high-performance I/O capabilities.

2.4 IRIO software library

IRIO software library has been designed with the goal of simplifying the interface with RIO devices. The access to FPGA resources is provided by NI-RIO Linux Device Driver. This Linux Device Driver provides a kernel module and a user space Library with the corresponding API. IRIO software library interfaces directly with NI-RIO Linux Device Driver and provides an API that simplifies the access to FPGA resources by other applications [3]. In this case, these applications are: the original IRIO library and NI-RIO EPICS Device Driver are defined by ITER and the additional function to processing the thermocouple signal is added to them for KoHLT-EB, as shown in Fig. 5.

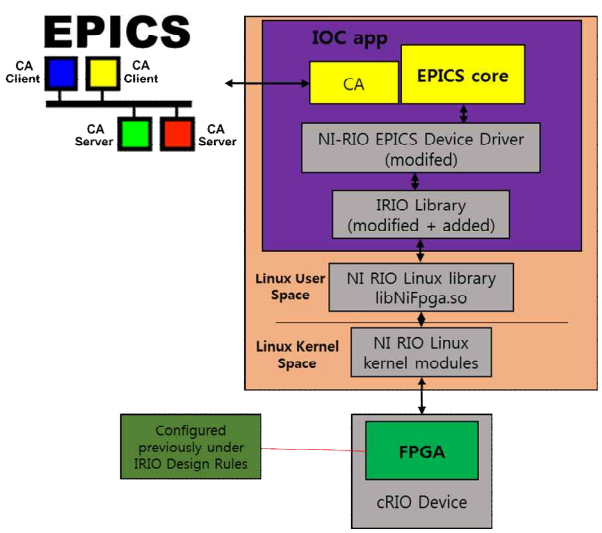

Fig. 5 Software layers used by modified Library

The cRIO module 9213 has a 36-terminal detachable sprint-terminal connector that provides connections for 16 thermocouple channels and supports high-resolution and high-speed timing modes. High-resolution timing mode optimizes accuracy and noise and rejects power line frequencies. High-speed timing mode optimizes sample rate and signal bandwidth. Fig.6 depicts the new DAQ system of KoHLT-EB that includes one 9205 and two 9213 module. Each 9213 module can be set high-resolution or high-speed mode in run-time.

Fig. 6 cRIO based DAQ system of KoHLT-EB

For cRIO devices the original IRIO library supports:

Table 1 cRIO devices supported by IRIO library

HW ID	Description
cRIO 9159	cRIO Chassis
cRIO module NI9205	Analog input Module
cRIO module NI9264	Analog output Module
cRIO module 9401	TTL Digital I/O
cRIO module 9477	Digital Outputs 60V sinking
cRIO module 9476	Digital Outputs 24V sourcing
cRIO module 9425	Digital Input 24V sourcing
cRIO module 9426	Digital Input 24V sourcing

But for the DAQ system of KoHLT-EB, IRIO library is modified then it also supports cRIO 9213 which is thermocouple input module.

3. Conclusions

The operator interface of KoHLT-EB DAQ system is composed of Control-System Studio (CSS), as shown in Fig. 7.

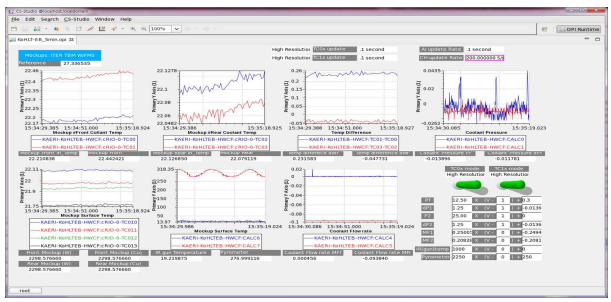

Fig. 7 OPI for KoHLT-EB DAQ system

Another server is able to archive the related data using the standalone archive tool and the archiveviewer can retrieve that data at any time in the infra-network, as shown in Fig. 8.

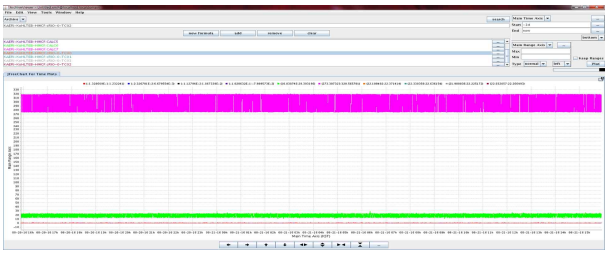

Fig. 8 archiveviewer

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[2] A. Bustos, M. Ruiz, Integration of a Data Acquisition System Based On FlexRIO Technology with EPICS, September 2014.
[3] IRIO Library user's manual.