# Design of a Loose Part Monitoring System Test-bed using CompactRIO

Min-seok Kim<sup>a\*</sup>, Kwang-Dae Lee<sup>a</sup>, Eui-Jong Lee<sup>a</sup>

<sup>a</sup>KHNP, Central Research Institute, 70, 1312-gil, Yuseong-daero, Yuseong-gu, Daejeon, 34101, South Korea <sup>\*</sup>Corresponding author: minseok2@khnp.co.kr

#### 1. Introduction

A loose part monitoring system (LPMS) is included in the NSSS integrity monitoring system (NIMS), which serves to detect loose parts in reactor coolant systems (RCS).

The main purpose of the LPMS is to provide an alert when an impact event occurs and to provide information to analyze the location, energy, and mass of loose parts [1].

LPMSs at Nuclear Power Plants (NPPs) in Korea follow the ASME OM standard and acquire data from 18 sensors simultaneously. Data acquisition requires a sampling rate of more than 50KHz along with a 12bit A/D converter [2].

Existing LPMS equipment is composed of several different platforms, such as a digital signal processor (DSP), a field-programmable gate array (FPGA), a micro control unit (MCU), and electric circuit cards. These systems have vulnerabilities, such as discontinuance due to aging and incompatibility issues between different pieces of equipment.

This paper suggests CompactRIO as a new platform. We devised a Test-bed using CompactRIO and demonstrate that the proposed method meets the criteria required by the standard.

#### 2. System Design

## 2.1 Overview of CompactRIO

CompactRIO (cRIO) is produced by National Instruments (NI). It is a rugged, reconfigurable industrial embedded system containing a real-time operating system (RTOS) and a FPGA chassis [3]. cRIO is designed for use in control and instrumentation equipment that must run high-speed real-time processes. Moreover, it is operable without a host PC.

There is an advantage when using various compositions of applications depending on how specific modules are connected to the FPGA chassis, as shown in Figure 1.



Fig. 1. Reconfiguration Embedded System Architecture.

Figure 2 shows the cRIO-9038 device, which uses a real-time controller and a FPGA chassis. It has redundant 9VDC to 30VDC supply inputs, a real-time clock, dual Ethernet ports, up to 2GB of storage, and built-in USB and RS232 support.



Fig. 2. NI CompactRIO cRIO-9038

The controller ensures in-time responsiveness because it operates in RTOS. Thus, it is a suitable system for implementing deterministic applications such as a LPMS.

The FPGA component refers to the chassis, which is used in connection with the controller. FPGA can implement correct timing in high-speed operations because the hardware operates independent of the OS.

## 2.2 Configuration of the NIMS Test-bed



Fig. 3. Configuration of the NIMS Test-bed

Figure 3 shows the configuration of the NIMS Testbed. An LPMS alarm processor was used for cRIO-9038, connected to a LPMS computer via a giga-bit Ethernet switch. Although cRIO-9038 has an Ethernet port, there is an additional Ethernet switch for the connection to the analysis computer and other systems of NIMS. The main components are shown in Table I.

| Items             | Description                  |
|-------------------|------------------------------|
| cRIO-9038         | FPGA: Xilinx Kintex-7        |
|                   | CPU: INTEL Atom 3825         |
|                   | OS: Real-Time Linux(64bit)   |
| AI Module NI-9215 | 16bit Resolution, 100kS/s/ch |
|                   | 4 Channel Differential Input |
| DO Module NI-9477 | 32 Channel Sinking Output    |
| DI Module NI-9426 | 32 Channel Sourcing Input    |
| Ethernet Switch   | Giga-bit Switch              |
| LPMS Computer     | CPU: I5-6, 2,3GHz            |
|                   | OS: Windows10                |

Table I : Components of the LPMS Test-bed

### 2.3 Performance Test of the LPMS Test-bed

Figure 4 shows the LPMS Test-bed with an added function generator for virtual sensor signals.

A Performance test was conducted in the real-time and event modes. The real-time mode uses a test that periodically shows a signal from 20 channel sensors on the screen of the LPMS computer. The event mode involves a test in which data are transferred and saved during 100ms from the alarm processor (cRIO-9038) to the LPMS computer when the measurement value exceeds a fixed or floating set-point.

The test involves a virtual sensor signal which is sent periodically to the AI module of the alarm processor. The Input signal is a sine wave ranging from 500 Hz to 20KHz on a 10-second cycle. The screen of the LPMS computer displays the test results. Figure 5 shows the test result in the event mode.

While the test is performed over several hours, highspeed signal processing and storage were successfully performed.



Fig. 4. Simulation of the LPMS Test-bed when an event occurs



Fig. 5. Screen Capture of the LPMS computer during an event analysis

## 3. Conclusions

The LPMS provides an alert when an impact event occurs and provides information with which to analyze the location, energy, and mass of the loose parts.

LPMSs in NPPs in Korea operate on a variety of platforms. Thus, these systems are vulnerable to discontinuances due to aging and incompatibilities arising from the use of different type of equipment.

In order to solve these problems, this paper suggests CompactRIO as a new platform. It is a rugged, reconfigurable, high-performance industrial embedded system. The results of performance tests meet the criteria set by the current standard.

In future work, the LPMS Test-bed will be optimized by the proper allocation of functions.

# REFERENCES

[1] Regulatory Guide 1.133, Loose Part Detection Program for the Primary System of LWRS, US NRC, 1981.

[2] ASME OM Standard Part 12, Loose Part Monitoring in Light-Water Reactor Power Plant, ASME, 2015.

[3] Developer's Guide, NI LabVIEW for CompactRIO Developer's Guide, NI, 2014.