FPGA-based 96-CH Digital DAQ system of Double-Scattering Compton Camera

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1. Introduction

The double-scattering Compton camera (DSCC) is a radiation imaging system which can provide both unknown source energy spectrum and 3D spatial distribution [1]. As shown in Fig. 1, the energies and detection locations measured in coincidence on three detectors contribute to computing Compton scattering angles and reconstructing emission energies and a spatial image based on conical surface integrals. We developed a FPGA-based digital data acquisition (DAQ) board of DSCC and tested the implemented functions of the FPGA-based DAQ such as interface calibration between 96 ADC channels and FPGA.

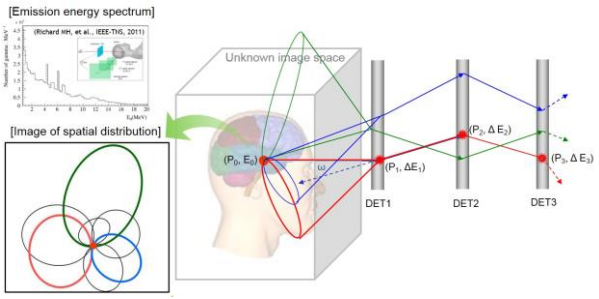

Fig. 1. Imaging principle of double-scattering Compton camera which operates on coincidence detection of three detectors.

2. Methods and Results

2.1 DAQ system of DSCC

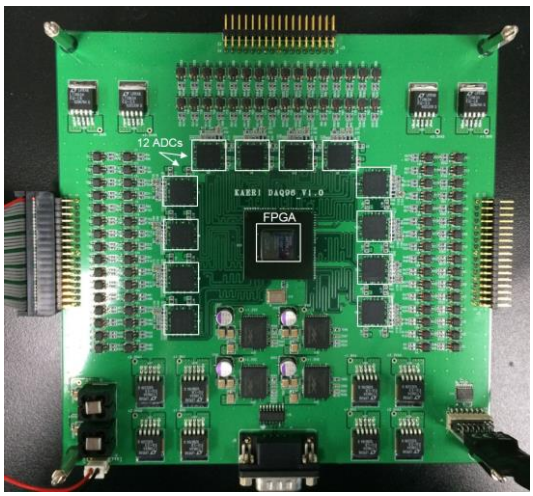

Fig. 2. DAQ board of double-scattering Compton camera consisting of 12 ADCs and FPGA.

In Fig.2, two main components in the DAQ system of DSCC are 12 analog-to-digital converters (ADC) and one field programmable gate array (FPGA). For ADC component, we used ADS-5281 which is an ADC having 8 channels and each ADC channel gives 12-bit serialized samples at 50 MSPS [2]. For FPGA, Artix7-200T was used [3]. The FPGA plays a role of controlling interface between ADC and FPGA, digital signal processing to extract detection information (energy and detection locations) from the measurements and coincidence detection, and transfer interface between FPGA and PC.

2.2 Interface between 12 ADCs and FPGA

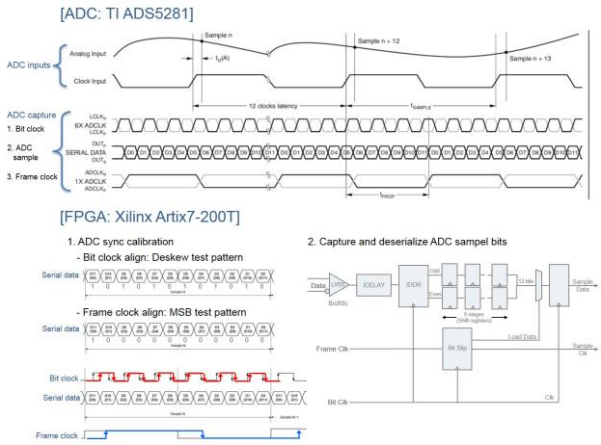

Fig. 3. Calibration diagram with Deskew and MSB test patterns to determine delay taps and bit slips for capturing 12-bit samples of 96 ADC channels.

In order to deserialize correctly the ADC sample bits arrived at FPGA into 12-bit parallel data, we need to align two bit and frame clocks to the serialized ADC sample bits. As shown in Fig. 3, we used two special test patterns, Deskew (010101010101) and MSB (100000000000) and then determined delay taps and bit slips of ADC bits from 96 channels to align bit and frame clocks. The delay taps applied to an IDELAY component of FPGA in Fig. 3 affect how long the ADC sample bits are delayed to capture the center of ADC bits at positive and negative edges of bit clock. Also the bit slip is related to capturing 12-bit parallel ADC data at positive edge of frame clock. Fig. 4 compares the deserialized ADC samples on analog Gaussian curve before (red curve) and after (blue curve) ADC calibration for one channel representatively. For all 96

ADC channels, the ADC calibration resulted in Gaussian curves of 12-bit ADC samples.

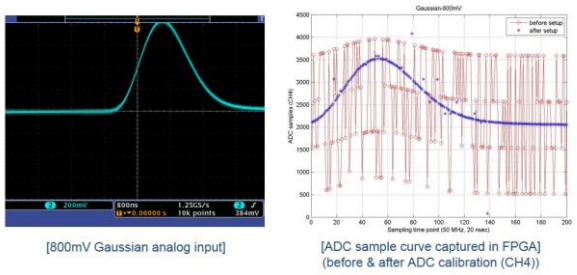

Fig. 4. Comparison of Gaussian ADC sample curve captured in FPGA before and after ADC calibration.

3. Conclusions

We developed a DAQ board consisting 96 ADC channels and FPGA and a calibration method of interface between ADC and FPGA using two special Deskew and MSB test patterns. The test results showed the interface between ADC and FPGA worked right after ADC calibration.

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