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Correlation between Guard Ring Geometry and Reverse Leakage Current of Si PIN Diode for Radiation Detector

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1. Introduction

Si PIN diodes were fabricated at the Radiation Equipment Fab. Center for direct measuring of low energy gamma/X-ray and coupling with scintillator for detecting high energy radiation [1]. There are many factors of Si PIN diode performance but one of the most important characteristic is low reverse leakage current for maximizing the signal to noise (S/N) ratio. Many efforts were carried out for low reverse leakage current for example, insert gettering layer [2], double deep diffused device structure [3] etc. In this paper, correlation between guard ring geometry and reverse leakage current of Si PIN diode were investigated.

2. Radiation Equipment Fab. Center

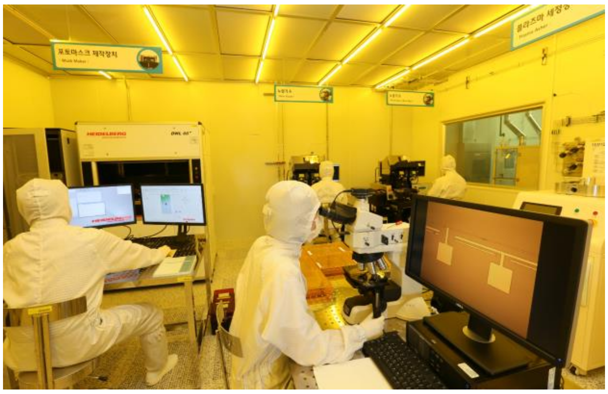

Fig. 1. Clean room for radiation sensor fabrication at Korea National Radiation Equipment Fab. Center.

The Radiation Equipment Fab. Center was built and full-scale operation was started from the Sep. of 2016. The purpose of the Radiation Equipment Fab. Center is invigorate of national radiation equipment research through set up the radiation generation/monitoring facility, performance test facility and relative equipment. Radiation Equipment Fab. Center targeting for creation of domestically producing infrastructure through commercialization as well as core technology research. Main application areas are radiation sensor, radiation survey meter, electron accelerator for medical/industrial use, container inspection system, radiation robot therapy, non-destructive inspection system for huge structure. One of the focused research area is Si PIN diode for room-temperature semiconductor radiation detectors (RTSDs). Semiconductor based CMOS process is possible in the fab. and wafer scale process optimization is in progress.

3. Methods and Results

3.1 Si PIN photodiode device Fabrication

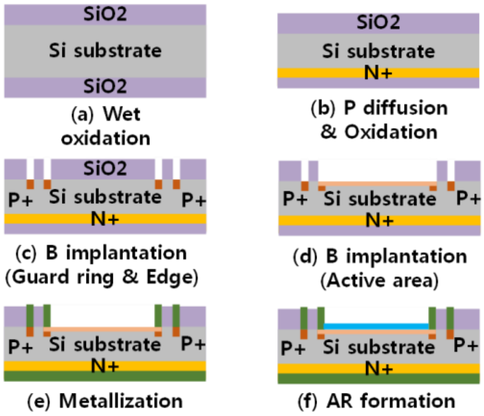

Fig. 2 Schematic process flow of Si PIN photodetector fabrication.

The fabrication process flow of Si PIN photodetector (1cm x 1cm) is schematically described in Fig. 2. Starting with the double side polished n-type high resistivity (>10 KOhm) Si substrate of (100) orientation, SiO_2 layer was formed by wet oxidation. Back side SiO_2 layer was removed and POCl diffusion process was carried out for N+ layer formation followed by protecting oxidation. After guard ring and edge area open by photolithography, ^{11}B implantation was performed for well formation. The implantation energy of ^{11}B was varied from 40, 60 and 80 keV for extracting correlation between guard ring depth and reverse leakage current. As higher the implantation energy, longitudinal and lateral straggling is getting bigger and deeper guard ring is formed. So, we can conclude that higher implantation energy makes bigger guard ring geometry. Second photolithography was carried out for active area open. After active area protecting oxide etch out, BF_2 was implanted followed by thermal activation. After metallization lithography, Al/Au was deposited by e-beam evaporation equipment and lift off was performed. Back side global metallization was also carried out and antireflection layer was deposited. Up to now, front-end process was completed and back-end process started. Wafer level device array was cut into single device by dicing machine and each device packaged to ceramic substrate with wire bonding equipment. Fig. 3 shows fabricated 10 mm x 10 mm Si PIN diode.

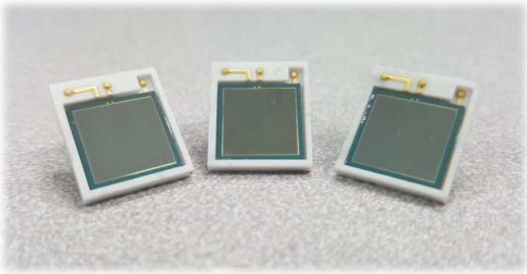

Fig. 3 Fabricated 10 mm x 10mm Si PIN diode.

3.2 Electrical Characteristics

Reverse leakage current is generally expressed the summation of four types of current as shown below equation [4]. I_{Leak} is the total leakage current, I_{DR} is the minority carrier diffusion current, I_G is the thermal generation current and I_{SR} is the surface current. As shown in the Fig. 4, I_{SR} and I_{INTER} is related to the guard ring which can push out the leakage current source.

$$I_{Leak} = I_{DR} + I_G + I_{INTER} + I_{SR}$$

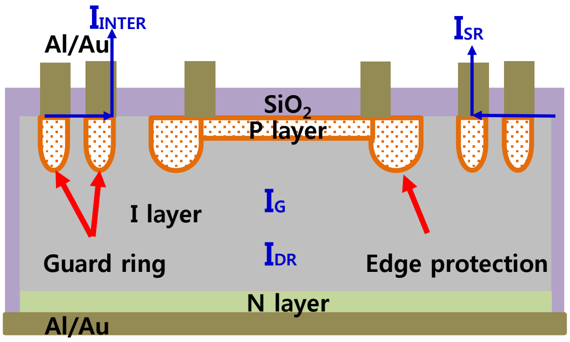

Fig. 4. Reverse leakage current source of double deep diffused structure of Si PIN diode.

Electrical measurement was performed by semiconductor parameter analyzer with probe station in the dark box. Reverse bias was applied from 0 V to -100 V with 0.1 V increment. Fig. 5 shows the leakage current versus reverse biased region of Si PIN diode according to ^{11}B implantation energy. ^{11}B implantation energy is directly related to the guard ring and edge protection well. For extracting correlation between guard ring/edge protection depth and reverse leakage current, ^{11}B implantation energy was varied from 40 keV, 60keV, 80keV and leakage current was 200nA, 65nA and 22nA at 70V respectively. Soft or hard breakdown was not observed up to -100V and leakage current was reduced as guard ring implantation energy is getting larger.

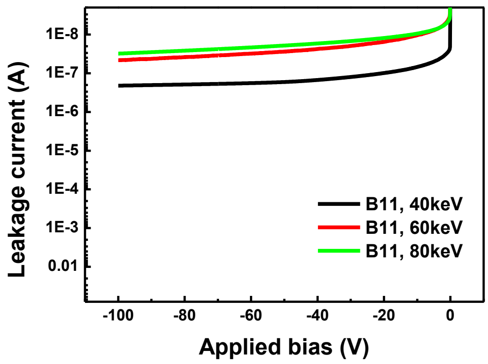

Fig. 5. I-V characteristics of Si PIN diode at the reverse biased region according to B11 implantation energy.

4. Conclusions

Lower leakage current at deeper guard ring device might be from effectively pushing out the I_{SR} and $I_{INTER.}$ Further optimization is needed to find out best guard ring implantation condition as well as whole fabrication process of Si PIN diode to reduce the reverse leakage current.

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