Radiation Hardening Techniques for Successive Approximation Register Analog to Digital Converter with Size Optimization and Layout

Seungho Jhung [a], Gyuseong Cho [a] and Inyong Kwon [b*]
[a]*Department of Nuclear and Quantum Engineering, Korea Advanced Institute of Science and Technology, 291, Daehak-ro, Yuseong-gu, Daejeon, Korea*
[b]*Korea Atomic Energy Research Institute, 111 Daedeok-daero 989 Beon-gil, Daejeon, Korea*
**Corresponding author: iykwon@umich.edu*

1. Introduction

Total Ionizing Dose (TID) effects and Single Event Effects (SEE) are the well known resultant effects on microelectronic devices and systems exposed to ionizing radiation. Many applications, such as aerospace and military electronics technology, have always encountered numerous occasions related to radiation interaction with matters. These fundamental challenges should carefully be considered when designing any radiation-hardened integrated circuits, especially for nuclear power plants (NPP) which requires high radiation hardness levels, in order to avoid parametric degradation and malfunction [1, 2, 5].

Radiation-Hardened-By-Design (RHBD) techniques have kept evolving for the past decades to satisfy the requirements of irradiating environment in NPPs; however, the possibilities of severe nuclear accidents still remain. To prevent and be well prepared for extreme events, advanced circuit designs reliable under harsh conditions are necessary.

Successive Approximation Register (SAR) Analog to Digital Converter (ADC) has advantages in regards to low power consumption and simple structure compared to any other types of ADCs. Recently, the enhancement of metal oxide semiconductor field effect transistor (MOSFET) operation speed has further lowered the limits of the conversion speed of SAR ADCs. Also, various schemes of calibration for nonlinearity issues are reducing capacitor sizes. The main purpose is to design SAR ADC that sustains performance under radiating environments by optimizing sizes of MOSFETs.

2. Background

In this section, radiation effects in MOSFETs are described for size optimization. This includes TID, SEE, and electronic noise.

2.1 Total Ionizing Dose (TID)

As shown in Fig. 1, when radiation is injected into MOS transistor, electron-hole pair (EHP) is formed inside the oxide layer and the holes are trapped due to their low mobility. This makes the MOSFET act like a normal transistor as if it is turned on, even though there is no gate voltage applied. The trapped charge built up in the gate oxide forms a conducting channel between the drain and source so that current -off current- flows,

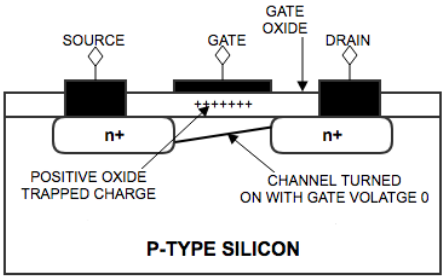

Fig. 1. Off current path formed between drain and source terminals.

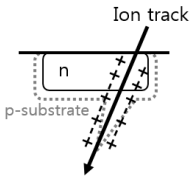

Fig. 2. Each heavy ion particle produces an ionization track

causing threshold voltage shift. If the voltage shift is large enough, the MOSFET resides in depletion mode, because of the leakage current path resulting in failure [3, 6, 7, 8].

2.2 Single Event Effect (SEE)

As shown in Fig. 2, high energy particle triggers SEE when entering an electronic device, creating EHPs along the ion track. The shape of the junction alters while these electrons and holes are relocated by the biased voltage, instantly switching the potential of the node. Then, the bit transition problem arises in digital circuits [4].

2.3 Electronic noise

Electronic noise is classified into two mechanisms: electron velocity fluctuations and electron number fluctuations. The electron velocity fluctuations corresponds to thermal noise, and the electron number fluctuations is represented by 1/f noise. Noise in MOSFET is expressed by

$$\frac{d\overline{e^2}}{df} = S_w + \frac{A_f}{f} = \frac{4k_BT\Gamma}{g_m} + \frac{K_f}{C_{OX}WLf} \quad (1)$$

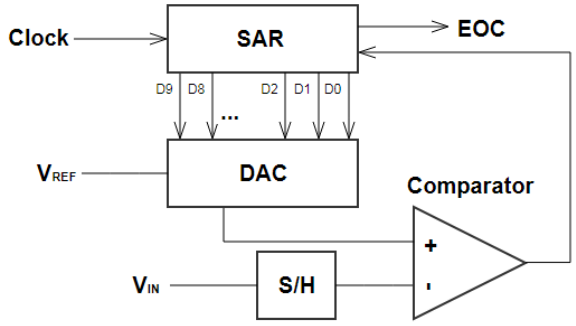

Fig. 3. 10-bit Successive Approximation Register Analog to Digital Converter block diagram

where $\overline{e^2}$ is a variance of a voltage source represented by means of power spectral density. $\frac{4k_BT\Gamma}{g_m}$, frequency independent term, is white noise (S_w) dominated by the channel thermal noise and consists of Boltzmann's constant (k_B), absolute temperature (T), channel thermal noise coefficient (Γ) and channel transconductance ($g_m \propto \frac{W}{L}$). The term, $\frac{K_f}{C_{OX}WLf}$, which is known as the 1/f noise or flicker noise, is inversely proportional to the frequency and consists of 1/f noise parameter (K_f), capacitance (C_{OX}) of the MOSFET and channel width and length (W, L). According to equation (1), it is possible to reduce the electric noise by increasing the channel width [5, 9].

3. Proposed Radiation Hardening MOSFET Size Optimization and Layout

3.1 Size optimized SAR ADC for Radiation Hardness

Optimizing MOSFET size is essential for designing a radiation hardening device. As shown in Fig. 3, a 10-bit SAR ADC is designed with 10 M/s sampling rate and 10μW of power. In addition, shortened channel length and broadened width of MOSFET size are reflected in the design, along with guard ring layouts, for radiation tolerance.

4. Conclusions

In the conference presentation, the proposed Successive Approximation Register Analog to Digital Converter size optimizations and layout for robust-to-radiation device will be discussed with initial simulation results. General aspects of the circuit are left unchanged, only simple modifications have been made, thus easily adaptable to radiation hardening applications. The entire circuit is in fabrication and will be tested.

This work was supported in part by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2017M2A8A4017932).

REFERENCES

[1] C. I. Lee, B. G. Rax, and A. H. Johnston, "Total Ionizing Dose Effects on High Resolution (12-/14-bit) Analog-to-Digital Converters", IEEE Trans. Nucl. Sci., vol.41, no. 6, Dec 1994.
[2] D. M. Fleetwood and H. A. Eisen, "Total-Dose Radiation Hardness Assurance," IEEE Trans. Nucl. Sci., vol.50, no. 3, Jun. 2003.
[3] T. R Oldham and F. B. McLean, "Total Ionizing Dose Effects in MOS Oxides and Devices", IEEE Trans. Nucl. Sci., vol.50, no. 3, Jun. 2003.
[4] T. R. Oldham et al., "SEE and TID Characterization of an Advanced Commercial 2Gbit NAND Flash Nonvolatile Memory", IEEE Trans. Nucl. Sci., vol.53, no. 6, Dec. 2006.
[5] R. Schwank et al., "Radiation Effects in MOS Oxides", IEEE Trans. Nucl. Sci., vol. 55, no. 4, Aug. 2008.
[6] V. Re, M. Manghisoni, L. Ratti, V. Speziali, G. Traversi, "Total ionizing dose effects on the noise performances of a 0.13 ㎛ CMOS technology", IEEE Trans. Nucl. Sci., vol. 53, no. 3, Jun. 2006, pp.1599-1606.
[7] N. S. Saks et al., "Generation of interface states by ionizing radiation in very thin MOS oxides", IEEE Trans. Nucl. Sci., vol. NS-33, no. 6, Dec. 1986.
[8] T. R. Oldham, "Ionizing Radiation Effects in MOS Oxides", World Scientific, 1999.
[9] H. J. Barnaby, "Total-Ionizing-Dose-Effects in Modern CMOS Technologies", IEEE Trans. Nucl. Sci., vol.53, no. 6, Dec. 2006.