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Radiation Hardening Techniques for a Preamplifier with Layout Strategy and Size Optimization

Changyeop Lee [a*], Gyuseong Cho [a] and Inyong Kwon [b]
[a]*Department of Nuclear and Quantum Engineering, Korea Advanced Institute of Science and Technology, 291, Daehak-ro, Yuseong-gu, Daejeon, Korea*
[b]*Korea Atomic Energy Research Institute, 111 Daedeok-daero 989 Beon-gil, Daejeon, Korea*
**Corresponding author: changyeop-lee@kaist.ac.kr*

1. Introduction

For many decades, various radiation-hardened-by-design (RHBD) techniques have been developed to meet the design requirements of irradiating environment in nuclear power plants. Improvements on the circuit side for radiation sensors in performance, chip size, and radiation hardening ability have been adopted in current plant systems; however, next generation reactors and/or preparation for severe events in existing reactors require advanced circuit structures that can provide relatively long viability in harsh conditions.

Preamplifier are essential components used to bridge two different signal-processing worlds between physical data from sensors and digital expression for human recognition. The positioning of preamplifiers should be coupled with sensors as close as possible to minimize any signal interference and noise. The location in or near a reactor pressure vessel requires radiation hardening techniques to prevent signal errors induced from radiation impacts on electronics that cannot be completely protected by standard radiation shielding techniques due to packaging, sizing, and high temperature issues. Therefore specialized RHBD techniques are required to protect circuits from radiation effects in those applications.

The proposed RHBD preamplifier could maintain its functionalities in harsh radiation environments at total ionizing dose (TID) rates higher than 1 Mrad. In addition, the specialized preamplifiers could be coupled with the new Micro Pocket Fission Detector (MPFD) of INL, resulting in a fully integrated fission detector module containing both sensor and readout circuitry that could be implemented immediately into existing nuclear power plants.

Generally, when radiation is injected into Metal Oxide Semiconductor Field Effect Transistor (MOSFET), Electron-Hole Pairs (EHP) are formed in the oxide layer and behaves like an insulator in the semiconductor, where it lead to changes in the device parameters due to trapped holes with low mobility inside the oxide layer. This results in TID which destroys the device, as Single Event Effect (SEE) also causes malfunction by triggering threshold voltage shift and leakage current. [2][3][8]

In this paper, modification of standard MOSFET layouts, Bipolar Complementary Metal-oxide Semiconductor (BiCMOS) circuit and variable channel length & width of MOSFETs suggest radiation hardening methods. These scheme have many strong advantages at using commercial MOSFET fabrications through simple active layer modifications without special fabrications such as Gate-Enclosed layouts MOSFETs, large gate MOSFETs.[11][12]

2. Background

In this section radiation affects in MOSFETs are described for size optimization. This includes threshold voltage shift and leakage current.

2.1 Threshold voltage shift

The threshold voltage shift is the result of charges trapped inside the oxide and the interface of a MOSFET.

First, the effect of the oxide-trapped hole, caused by injected radiation, is expressed by

$$\Delta V_{OT} = -\frac{q}{C_{OX}}\Delta N_{OT} = -\frac{q}{\varepsilon_{OX}} t_{OX}\Delta N_{OT} \quad (1)$$

where q is elementary charge, and C_{OX} is the specific capacitance of the MOS capacitor. ΔN_{OT} is the density of oxide-trapped holes per area unit, given by $\Delta N_{OT} = \int_0^{t_{OX}} n_{th}(x)dx$. According to this equation, ΔV_{OT} is proportional to t_{OX}^2. [8][9]

Second, interface-trapped holes change the MOSFET channel charges given by

$$\Delta V_{IT} = -\frac{\Delta Q_{IT}}{C_{OX}} \quad (2)$$

where ΔQ_{IT} is the interface-trapped charges, which breaks the channel charge balance, dependent on the type of MOSFET.

The overall threshold voltage shift is expressed by[11]

$$\Delta V_{OV} = \Delta V_{OT} + \Delta V_{IT} \quad (3)$$

Therefore, minimizing t_{OX} is essential in order to make radiation hardening devices.

2.2 Leakage current

The field oxide, used to electrically isolate devices, has the thickness ranging between 100 and 1000nm.[4] For N-channel Metal Oxide Semiconductor (NMOS) of Fig. 1, trapped holes in the field oxide due to ionizing radiation can create the N-type conducting channel between the drain and source terminals.

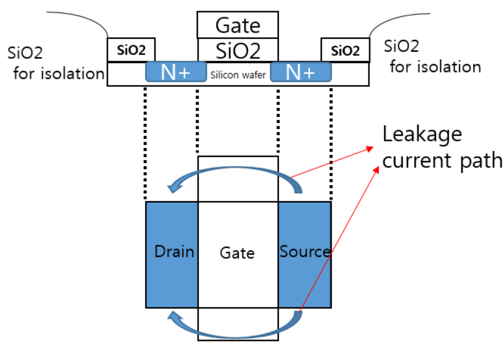

Fig. 1. Formed leakage current path between drain and source terminals.

On the other hand, the leakage current in P-channel Metal Oxide Semiconductor (PMOS) cannot flow as much as NMOS because the channel charges are carried by holes.[5]

3. Proposed Radiation Hardening Layout and Size Optimization

3.1 Proposed Radiation Hardening Layout

As mentioned above, in order to minimize the effect of both threshold voltage shift and leakage current, reducing the thickness of the SiO2 layer is important. For this reason, deep-submicron CMOS technologies have robustness to TID.[7] This is because quantum tunneling of electrons in the thin gate oxide makes most of the generated holes caused by induced radiation recombination, leaving only few to be trapped.[1] Fig. 2 shows an original N-type MOSFET layout of standard cell that is fabricated with broader implantation area than active area. Active area designates thin gate oxide which has thickness ranging between 1 and 3nm.[4] The proposed N-type MOSFET layout of Fig. 3 conjugates broad active area to avoid threshold voltage shift and leakage current.

3.2 Size optimized Preamplifier and BiCMOS for Radiation Hardness

MOSFET size optimization is essential when designing a radiation hardening device, such as reducing electric noise with increasing channel width. [10] Generally, p-type MOSFET device has radiation hardening characteristics because major charge is holes. Additionally, for Bipolar Junction Transistors (BJT), the leakage current of the n-types is lower than the p-types due to the BJT structure.[6] Therefore, in this paper preamplifier with various channel length and width are used and a BiCMOS preamplifier is designed as shown Fig. 4.

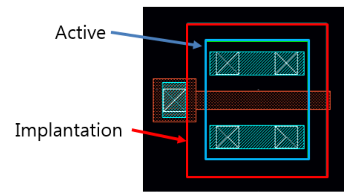

Fig. 2. A Original standard N-type MOSFET layout of commercial fabrication

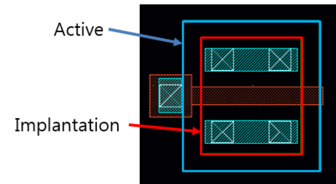

Fig. 3. Proposed radiation hardening N-type MOSFET layout with broadened Active area

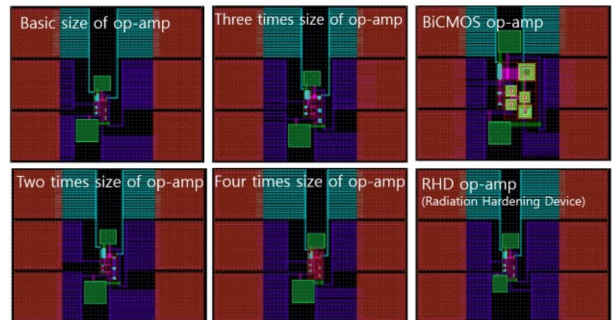

Fig. 4. Preamplifier layout with variable size and proposed radiation hardening layouts

4. Conclusions

In this paper, the proposed MOSFET layout and size optimizations for, robustness to radiation, are presented. Furthermore, the proposed MOSFET layouts provide advantages in simple modification from the standard fabrications, simply adaptable for radiation hardening integrated circuit applications in terms of threshold voltage shift and leakage current. The entire circuit is in fabrication and will be tested. This work was supported in part by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2016M2A8A1952801).

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