Design of the Low-Noise Charge Sensitive Preamplifier for Semiconductor Radiation Detectors

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1. Introduction

Semiconductor radiation detectors such as CdZnTe, HgI_2 and photodiode become increasingly important because of their compactness and room temperature operation etc. In spite of their advantages, they suffer from noise that arises from various readout components due to their too small signal level. Noise of the readout circuits in the radiation detection is a critical factor that affects the performance of the circuits. The magnitude of the noise determines the lowest limit of the signal size that can be handled by a circuit without significant deterioration in the original signal. The energy resolution of a spectroscopy system or the image quality of 2D pixel arrays is deeply related to the noise of readout circuits. In the design of such electronics system, it is very important to optimize the noise performance of preamplifiers, since in a well-designed system the noise performance of the entire system is always dominated by the preamplifier noise [3]. In this study, two types of CSA (Charge Sensitive Preamplifier) with different input transistors were designed for semiconductor radiation detectors.

2. Methods and Results

2.1 Circuit Design

The CSA was designed with folded cascade structure using the AMS 0.8 μm CMOS process [2]. Two kinds of CSAs were implemented with the different size of the input transistors, which have a ratio of 1:2. The channel length of the input transistors is fixed to the minimum feature size for all the CSAs.

Shown in Fig. 1, the input stage was composed of differential pair with NMOS and PMOS in order to increase input dynamic range. The input signal is amplified through the differential pair with M9/M11 and M10/M12 transistors. The amplified signal is delivered to second amplifying stage with four auxiliary amplifiers. Each amplifier has folded cascade structure and inverting configuration. The Aux_p and Aux_n receive output signals from NMOS and PMOS differential pair respectively. M3/M4 and M7/M8 transistors are an output stage. The Diff_Bias and POR make up the bias generator that supplies the folded cascade stage with bias voltage. The CMFB (Common Mode Feedback) has the DC bias voltage of the output stage maintained uniformly.

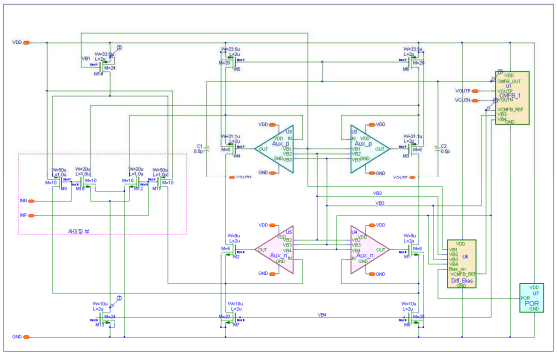

Fig. 1. Schematic diagram of the charge sensitive preamplifier circuit with folded cascade structure.

2.2 Simulation Results

The CSA circuit was designed through circuit simulation using HSpice that is integrated circuit simulator. The model parameter supplied by process foundry was used for simulation. In Fig. 2, the simulation results for CSA are shown. As a result of AC analysis, the open loop gain is 130 dB, the gain bandwidth is 22 MHz and the phase margin is 58 degree.

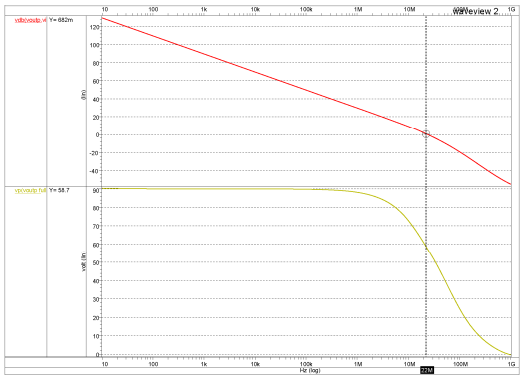

Fig. 2. Simulation results of AC analysis for the designed CSA.

2.3 Layout and Fabrication

To fabricate the CSAs, the layout of the masks was drawn and the DRC (Design Rule Check) was performed. The result of the layout is shown in Fig. 3. The CSA test chips were fabricated using AMS 0.8 μm CMOS process through a MPW (Multi-Project Wafer) supplied by EUROPRACTICE [1]. This CSA is operated at 5V. The feedback capacitor and resistor can

be changed to any values externally. The fabricated CSA test chip is shown in Fig. 4.

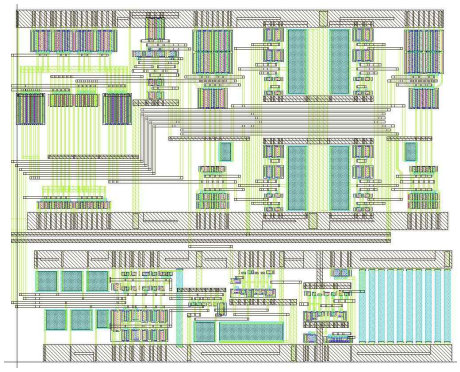

Fig. 3. Layout of the CSA.

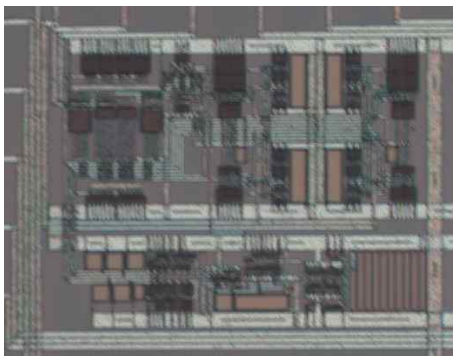

Fig. 4. Photograph of one of the CSA test samples fabricated using AMS 0.8 μm CMOS process.

3. Conclusions

Two kinds of low-noise CSA with different input transistor size were designed and fabricated using AMS 0.8 μm CMOS process. The CSA is composed of differential paired input stage and folded cascade amplifying stage. To optimize the performance of the circuits, HSpice was used for simulation and the results are A=130 dB, fT=22 MHz and PM=58˚.

ACKNOWLEDGMENT

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