Full-Core Pin by Pin Subchannel Analysis of SMART

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1. Introduction

MATRA-S[1], a subchannel analysis code was modified to analyze full-core of SMART with pin by pin subchannel model without lumping channels. The SMART core has 57 fuel assemblies of 17x17 arrays with 264 fuel rods and 25 tubes and there are total of 15,048 fuel rods and 16,780 subchannels as shown in Fig.1.

Subchannel analysis of a whole reactor core usually has modeled by lumping channels. It lumps several subchannels or assemblies into a big virtual channel and reduces a number of channels and a calculation size of the problem by more than few orders of magnitude. The subchannel analysis models for evaluation of thermal margin of SMART core[2] are 44 and 39 channels for the 1/8-symmetry core as show in Fig.2. The models were developed to be simple that they can be evaluated within reasonable time but to be conservative to a reference model. The reference model is a pin by pin 1/8-core subchannel analysis model and it has 2,333 subchannels and total of 2,119 fuel rods and tubes. The lumped models adopted several engineering factors and assumptions for conservativeness.

As the computing power increases drastically, a single stage, full core pin by pin subchannel analysis has become true. This full real subchannel analysis model can obtain more operating margins than lumped models if it is applicable within reasonable time and cost.

2. Subchannel Analysis Models

Even though the computing power is increased, cost of full core pin by pin analysis is expensive and is time consuming. The MATRA-S code was modified totally for full core calculation and optimized for calculation speed. The code was re-constructed to handle a very large problem such as more than 60,000 fuel rods and 70,000 subchannels.

Many needless common variables were converted to local variables or removed. A total memory size required for a computation was minimized by reduction of common variables and conditional dynamic memory

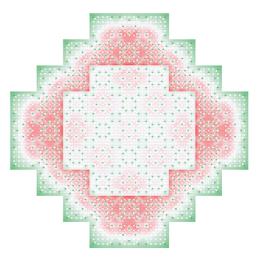


Fig.1. A Sample of Pin Power Distribution of SMART

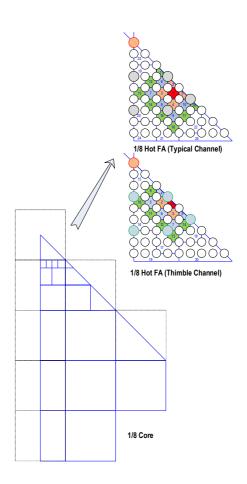


Fig.2. Lumped Models for 1/8-Core of SMART

allocation of only necessary common variables as shown in Fig.3.

Bottle necks of the MATRA-S code were searched through performance profile analyses and the parts were modified for speed-up, i.e., a subroutine DIVSOR that solves linear and lateral momentum combined equation consumed more than 55% of total calculation time before optimization, and it was reduced to less than 20% after optimization for a 2,333 channel problem of 1/8-core as shown in Fig.4.

A computation time of subchannel analysis for a full core in Fig.1 is about 3 hours whereas it takes only a few seconds for the lumped model for 1/8-core on an Intel[®] Core[™] i7-860 computer. some iterative methods such as a BiCGSTAB and a full GMRES of Krylov subspace were implemented and a library SuperLU was adopted to solve the linear and lateral momentum combined equation in order to improve the calculation efficiency. Benchmark tests for these iterative methods are in process. Another effort for improvement, loop unrolling was tried manually but there were no significant difference between automatic loop unrolling by the Intel[®] Fortran compiler.

3. Conclusion

The MATRA-S code was modified and optimized successfully to calculate full core pin by pin subchannel analysis model for SMART. The code can handle a very large problem with more than order of 10⁵ channels. The full core analysis takes more than 3 hours and it is not realistic for core design such as a thermal margin analysis. And some iterative methods such as a BiCGSTAB and a full GMRES of Krylov subspace were implemented and a library SuperLU was adopted in MATRA-S and benchmark tests are under test to improve calculation speed for the full core pin by pin subchannel analysis model.

The single stage full core analysis may help securing more operation margin and economic efficiency by reducing many engineering factors and assumptions that were applied to previous lumped subchannel analysis model.

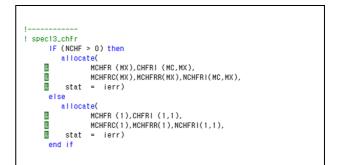


Fig.3. A Sample of Memory Reduction

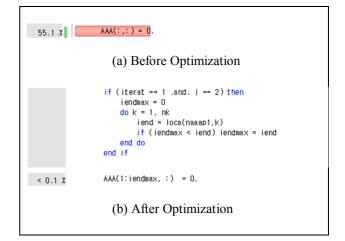


Fig.4. A Sample of Code Optimization for Speed-up

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