A 10-bit Radiation-Hardened R-2R Digital-to-Analog Converter for Nuclear Power Plant Applications

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1. Introduction

In order to cope with severe accidents as soon as possible such as the Fukushima case, the importance of controlling and monitoring analog devices in Nuclear Power Plant (NPP) has increased [1]. For example, as an interface between analog and digital, Digital-to-Analog Converter (DAC), which converts the digital expressions ("0" or "1") to the analog value of a continuous amplitude, is one of the non-replaceable electronic components controlling various analog equipment (eg. valves in NPPs).

Unfortunately, as we have experimented in Fig. 1, most commercial DAC chips lose its functionality in high-level radiation environments which can be caused in reactor leakage accidents [2-4]. Fig. 1 shows a result of two DAC chips (Analog Device, AD5433) irradiation test. The amplitude of the DAC should be toggled to the preset analog voltage value every hour, but irregular signals were occurred after about 800 Gy of Total Ionizing Radiation Dose (TID) irradiated by 1.05 kGy/h with ^{60}Co.

In those harsh radiating environments, electronics could malfunction due to the TID effect. Over the past decades, it is well known that TID effects can cause functional degradations and failures in integrated circuits. These effects occur when electron-hole pair (EHP) are generated by ionization radiation. The holes of EHPs can be trapped in gate oxide or Shallow trench isolation (STI) regions because of its lower mobility rather than electron inside those regions. Due to this hole trapping mechanism, threshold voltage of the device shifts and leakage current increases [5].

In order to mitigate such a severe TID effect, a lot of DAC design techniques considering space field dose rate have been proposed [3-4]. Although these approaches are performed well, errors could occur at higher harsh environments (above 1 kGy) than aerospace exploration.

In this work, by considering these extreme radiation environments, we are reporting integrated circuit design techniques and simulation results for a 10-bit radiation-hardened R-2R DAC. The R-2R resistor ladder structure selected in this study is more robust than other DAC structures for its simplicity and using less active component. It also consumes low power [4].

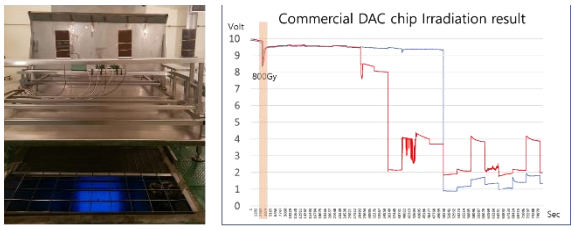

Fig. 1. (a) Photo of the irradiation test setup in the gamma irradiation facility with ^{60}Co of KAERI, and (b) irradiation test results of the commercial DAC chips.

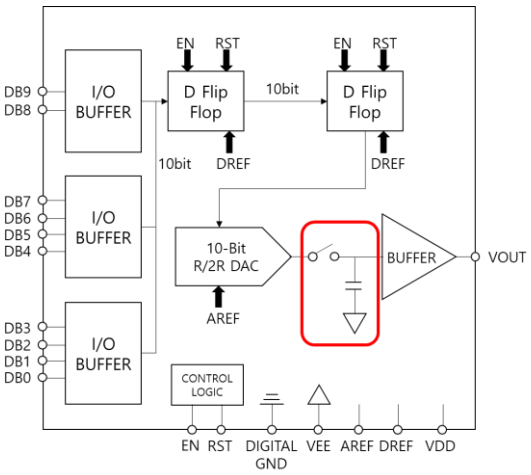

Fig. 2. The overall structure of the proposed 10-bit radiation-hardened DAC.

2. Configuration of the proposed technique

The overall structure of the proposed 10-bit radiation-hardened R-2R DAC is shown in Fig. 2. This system is divided into the digital and the analog parts. The digital block consists of I/O buffer, D Flip Flop and control logic. These are supplied reference voltage by DREF port. When the digital data (DB0 ~ DB10) is applied, the input signal is transferred to the D Flip Flop through the I/O buffer composed of inverters and it is latched or transferred as an enable signal for the control logic.

The digital output of D Flip Flop is converted to an analog signal in 10-bit R-2R DAC block. In order to improve the matching and linearity, all the resisters used in the R-2R ladder are integer multiples of a base size one. The analog output range can be controlled through AREF external terminal. The output of R-2R DAC, converted to an analog signal, is connected directly to

analog buffer which has the high-input-impedance and low-output-impedance to minimize the load effect. This buffer output is connected to the VOUT terminal. The red box in Fig. 2 have not yet been applied to this paper and will be explained with simulation result in section 3.

The digital components used in this structure could be more tolerant against TID effect than analog circuits because it is only required to express "0" or "1", the limitation of the linearity is less as well as the electronical margin is higher than the analog component. It is proven that the digital inverters fabricated in the 180 nm CMOS process had not a functional problem at total radiation dose about 35 kGy although it had a slight shift in threshold voltage [6]. Therefore, we did not add any special design techniques to the digital parts.

Unlike the digital blocks, the analog buffer is the most challenging parts of radiation hardened DAC. Typically, the buffer is designed as an operational amplifier with a feedback resistor which controls the gain to determine whether to use it as a buffer or an amplifier [3, 4]. Those operational amplifiers are more susceptible to TID effects than digital blocks because threshold voltage shift, even a slight shift, could seriously affects the saturation region of the current source as well as operating point change. Subsequently, TID effect could makes the amplifier disable.

In this work, we have replaced this amplifier with a source follower which has a small number of MOSFETs and only operates as a buffer shown in Fig. 3. Q1 is the current source, Q2 and Q3 are the current mirrors and act as an active load. D1 improves the input range of Q4 by biasing as much as the threshold voltage of Q4. The input and output range of source follower is 0 to 2V.

In addition, for preventing TID effect caused by the hole trapping in the high radiation environment, we chose the transistor length within 350 nm because the threshold voltage shifts caused by fixed oxide trapped charge buildup are proportional to the square of oxide thickness as following equation [5]:

$$\Delta V_{ot} = -\frac{t_{ox}}{k_{ox}\varepsilon_0} q\Delta N_{ot}, \qquad (1)$$

where ΔV_{ot} is threshold voltage shift, k_{ox} is the dielectric constant of SiO_2, ε_0 is the permittivity of free space and ΔN_{ot} is proportional to the thickness of the oxide.

3. Preliminary Simulation Results

Fig. 4 shows the simulation results of a 10-bit radiation-hardened DAC. The top of the picture is the reset signal and bottom is the output signal of DAC. We confirm that VOUT linearly increases 0 to 2V as the input digital value increases and successfully reset when the reset signal is switched to high. The conversion time of Least Significant Bit (LSB) is applied 10 ns.

As shown in bottom of fig. 4, glitches are occurred when the MSB changes as the digital value increase (major carry transition). To alleviate these glitches and hold the existing analog signal for a while, we plan to add the hold capacitor and digital logic switch synchronized with the MSB are used at the end of the R-2R DAC as the red box in Fig. 2.

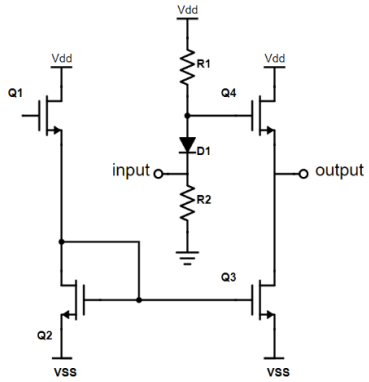

Fig. 3. The source follower with active load schematic. It can be a simple replacement for complex amplifier.

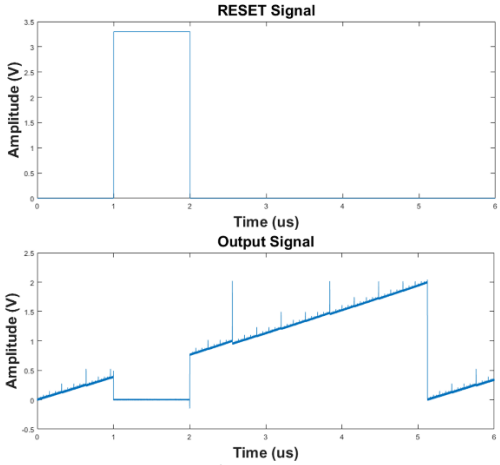

Fig. 4. Simulation results of a 10-bit radiation-hardened DAC.

4. Conclusion and Future Work

In this study, we have designed a 10-bit radiation-hardened DAC using R-2R structure and simulated the linearity and control logic as the digital input. The output range of this DAC is 0 to 2V. The main feature of this system is that the source follower is used instead of the complicated amplifier and the length of each transistors is designed to be less than 350 nm in order to minimize the influence of TID.

Between now and the conference presentation, we plan to complete the overall layout, then fabricate integrated circuit through the standard CMOS 180 nm process. After the chip is verified the basic parameters, Differential Non-Linearity (DNL), Integral Non-Linearity (INL), etc., the irradiation test will be performed at the gamma-ray facility with ^{60}Co in KAERI. In this test, we will measure the output voltage and power supply current to verify the operation performance of the DAC as well as other figure of merits.

Acknowledgements

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