Analysis on Static Noise Margin of 10T SRAM for Radiation Tolerance

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1. Introduction

In the space environment, a common problem in memory semiconductors is soft errors. The main cause of soft errors is Single Event Effect (SEE) caused by radiation, which means that a single active particle additionally generates electric charges or current inside the semiconductor chip, resulting in malfunction [1].

Static Random Access Memory (SRAM) is a memory device of which cell consists of inverters. It can retain its stored information as long as power is supplied. Also, it has some advantages in fast processing speed and minimum power consumption. However, SRAMs are also vulnerable to radiation, especially when single event upset (SEU) occurs [2]. The SEU is a type of SEE that makes bits inverted. Therefore, it is critical for SRAM and must be considered when designing.

In this study, we propose a new 10T SRAM structure (added a tri-state buffer to conventional 6T SRAM) which has stronger radiation resistance, and compare the performance with the conventional 6T SRAM structure by simulations.

2. Conventional 6T SRAM

2.1 Operation

• Read mode

First, the WL (word line) is given a LOW signal to turn off the access transistors. Then BL (bit line) and BLB (bit line bar) are precharged by half of VDD. When the access transistors are turned on by giving HIGH signal to WL again, the values stored in nodes Q and QB are transmitted into BL and BLB. Finally, it is amplified by a sense amp at the end of BL and BLB [3].

• Write mode

In contrast to the read operation, initially turn on the access transistors by applying a HIGH signal to the WL. BL must get HIGH signal for writing HIGH to memory, and LOW signal for writing LOW. Finally, turning off the access transistors by giving the LOW signal to the WL ends the operation and keeps the memory value until next writing [3].

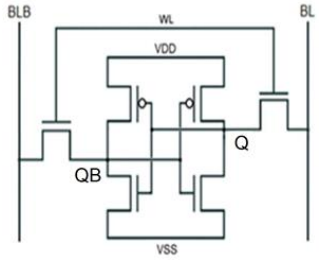

Fig. 1. Schematic diagram of the conventional 6T SRAM cell

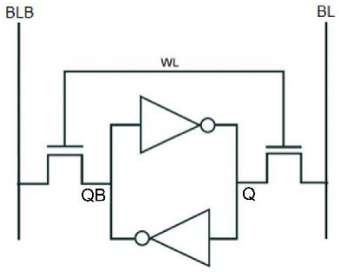

Fig. 2. Block diagram of 6T SRAM cell

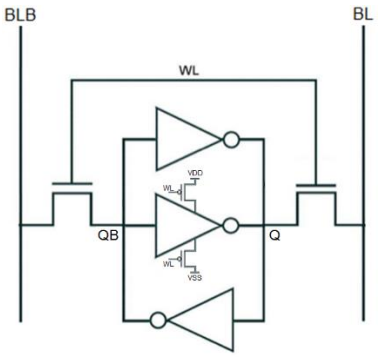

Fig. 3. Block diagram of 10T SRAM cell

2.2 Single Event Upset

To consider the SEU, the initial value of Q and QB should be referred. If the induced current by radiation is injected to these sensitive volumes, the bit of affected node is changed due to the influence of radiation, and then the other is instantly changed along. Therefore, the bit is easily flipped by the radiation in 6T SRAM cell.

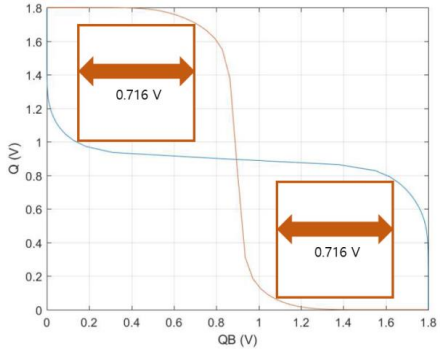

Fig. 4. READ SNM of Conventional 6T SRAM

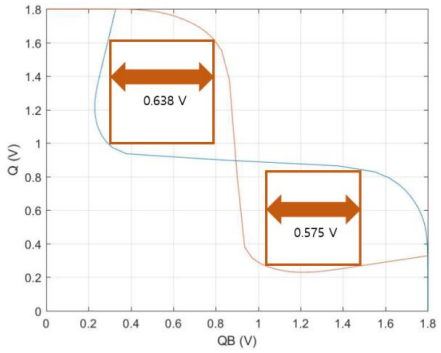

Fig. 5. WRITE SNM of Conventional 6T SRAM

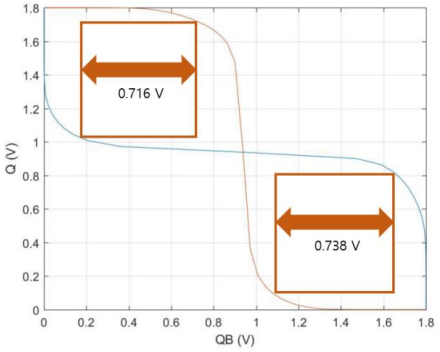

Fig. 6. READ SNM of 10T SRAM

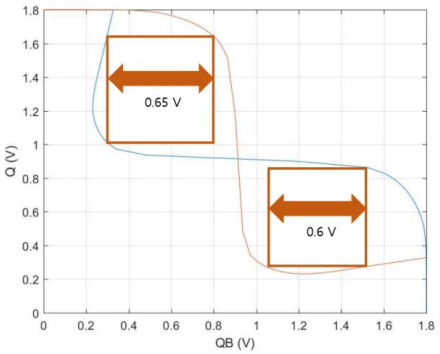

Fig. 7. WRITE SNM of 10T SRAM

3. Proposed 10T SRAM

Proposed 10T SRAM consists of three inverters in parallel. One of them is a tri-state buffer with a pmos switch at the top and bottom of the inverter, and it raises the drive strength. As a result, a 10T SRAM can hold memories after irradiated for a longer time than 6T SRAMs. So, it has better durability to radiation effects.

4. Simulation Results of 6T and 10T SRAMs

SNM is one of the indicators to determine the stability of SRAM operation. The data in SRAMs with large SNM values are not easily reversed despite the large noise, which means that the data is stored stably. Conversely, as the SNM approaches zero, it means that the operation is unstable because data is easily overturned even with very small noise [4].

As shown in figures, READ SNM is 0.716 V for conventional 6T SRAM and 10T SRAM in simulation results (Fig. 4 and 6). Interestingly, one side of readout nodes show better noise margin of 0.738 V thanks to the additional circuit in the cell as noted in Table I. And, the WRITE SNM of the 10 T SRAM is 0.575 V which better than one of the 6 T SRAM of 0.6 V (Fig. 5 and 7). It can be seen that 10T SRAM is more stable than conventional 6T SRAM. Furthermore, it also has higher hardness to SEE as well as noises.

TABLE I. COMPARISION OF 6T AND 10T SRAM

SRAM	Transistors	Read SNM	Write SNM
6T	6	0.716 V	0.575 V
10T	10	0.716 V (0.738 V)	0.6 V

5. Conclusions

For memory semiconductor devices such as SRAM, soft errors must be considered for harsh radiation environments. So, we proposed a new 10T SRAM structure which has additional tri-state buffer compared to conventional 6T SRAM. Prior to design, it was assumed from the block diagram that a 10T SRAM can hold memories for a specific time and this time is longer than that of 6T SRAM. But the performance simulation results were same. As a result, proposed 10T SRAM has higher the SNM value, which indicates the stability of the SRAM operation, than the conventional 6T SRAM in writing.

In the ongoing study, we are finding out the threshold LET value to see how much radiation energy the 10T SRAM cell can stand and comparing that value with 6T SRAM.

Acknowledgements

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REFERENCES

[1] G. Toure, J. -. Portal, G. Hubert, K. Castellani-Coulié and A. Lesea, "Effect of multiple injections on the SEEs in SRAM cell," *2009 European Conference on Radiation and Its Effects on Components and Systems*, Bruges, 2009, pp. 252-255.
[2] F. Vargas and M. Nicolaidis, "SEU-tolerant SRAM design based on current monitoring," *Proceedings of IEEE 24th International Symposium on Fault- Tolerant Computing*, Austin, TX, USA, 1994, pp. 106-115.
[3] A. Bhaskar, "Design and analysis of low power SRAM cells," *2017 Innovations in Power and Advanced Computing Technologies (i-PACT)*, Vellore, 2017, pp. 1-5.
[4] A. Sil, S. Ghosh, Neeharika Gogineni and M. Bayoumi, "A novel high write speed, low power, read-SNM-free 6T SRAM cell," *2008 51st Midwest Symposium on Circuits and Systems*, Knoxville, TN, 2008, pp. 771-774.