Component Test of Processor Module PLD Logic for Safety-grade PLC

Ka-Ram Park [a*], Kwan-Woo Yoo [a], Dong-Yeon Lee [a]
[a]*SOOSAN ENS Co., Research Institute, 3F, Suseo Hyundai Ventureville, 10, Bamgogae-ro 1-gil, Gangnam-gu, Seoul, 06349*
[*]*Corresponding author: psh6514@soosan.co.kr*

1. Introduction

These days, Nuclear power plant is devoting a lot of effort to replace most of the instrumentation and control systems from analog to digital [1]. The digital instrumentation control system is an important system that directly affects the safety of nuclear power plant [2]. Therefore, it is very important to design and verify the safety-grade PLC (Programmable Logic Controller) for system control. In order to ensure high reliability and high stability of safety-grade PLC, it should be designed according to the Code & Standard [3]. It is then essential to check the design by performing verification & validation [4]. This paper describes a component test for verification of POSAFE-Q processor module PLD (Programmable Logic Device) logic named NLCPU2 that meets the requirements of Safety Class 1E.

2. Component Test Objective

In this section it is described with respect to how to select the test items and how to extract test cases.

2.1 Test Items

The test is performed to verify that all functions described in the SDS (Software Design Specification) of NLCPU2 are implemented [5]. So the test items are targeted at all functions in the SDS of NLCPU2. The functions designed in the SDS of NLCPU2 are shown in the figure 1.

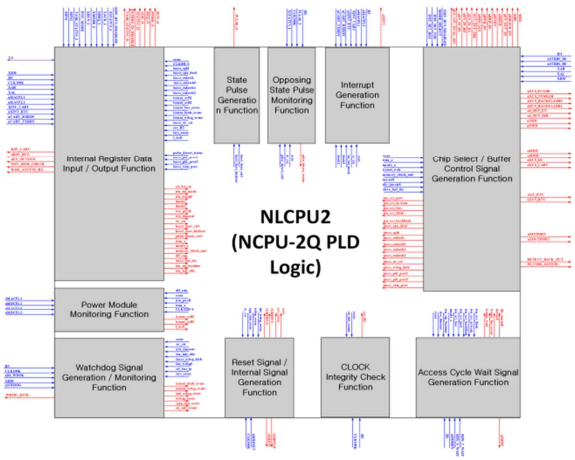

Fig. 1. Signal connection diagram between NLCPU2 function parts.

2.2 Test Case Extraction

The features of NLCPU2 that is implemented based on SDS are extracted, and it creates cases that can test all the extracted features. Each test case consists of a test input and an expected output for the test input. All detailed functions described in SDS should be tested at least once.

3. Component Test Method

In this section it is described for component test approach, test environment, and test procedure.

3.1 Test Approach

The features of NLCPU2, which are designed through development artifacts, are identified, and the test bench that includes all test cases extracted from SDS is designed. The test verifies functions of the NLCPU2 designed in VHDL (VHSIC Hardware Description Language) through the ModelSim simulation method. Figure 2 shows an overview of the overall component test.

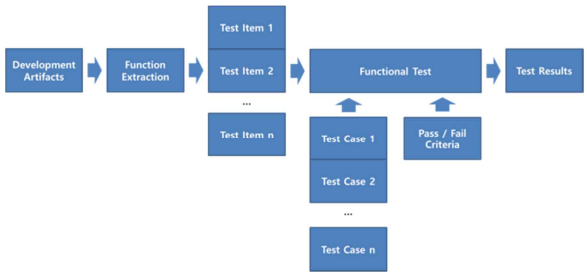

Fig. 2. Overview of the component test.

3.2 Test Environment

The HOST-PC used for the test is equipped with software programs that are ModelSim, Project Navigator (ISE 14.7), and Windows 7. Figure 3 shows the test environment configuration used for the NLCPU2 simulation test.

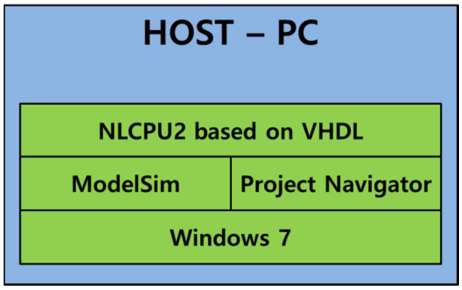

Fig. 3. Test environment configuration.

ModelSim is a software tool that can simulate PLD logic designed with VHDL. Project Navigator is a software tool for designing Xilinx's CPLD (Complex Programmable Logic Device) and FPGA (Field Programmable Gate Array).

3.3 Test Procedure

First, the expected output signal when the test input signal for each test case is applied to the implemented NLCPU2 is written. Figure 4 shows the test input signals and expected output signals of the F_CT_M_01 test case.

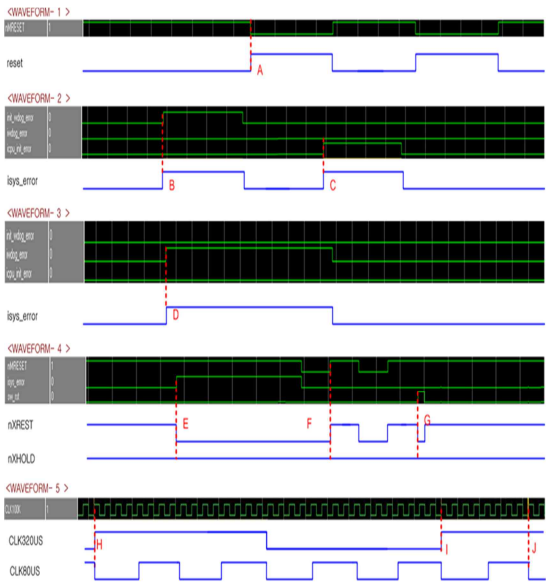

Fig. 4. The test input signals and expected output signals of the F_CT_M_01 test case.

The actual output signal is verified through the designed testbench simulation, and whether the test is passed or not is determined by comparing the actual output signal with the expected output signal. Figure 5 shows the actual test output results of the F_CT_M_01 test case, and that the actual test results are the same as the expected output signals.

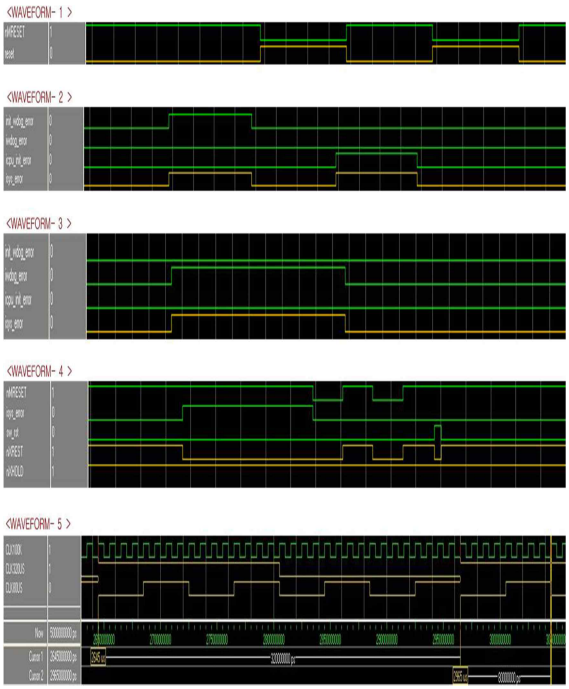

Fig. 5. The actual output signals of the F_CT_M_01 test case.

In such cases, the results of the test are determined by pass and the following test cases are carried out. Table I shows the results of F_CT_M_01 test case.

Table I: Results of F_CT_M_01 test case.

Test Case	F_CT_M_01
Signal Name	nMRESET sw_rst icpu_init_error iwodg_error init_wdog_error
Expected Output	nXREST nXHOLD reset isys_error CLK320US CLK80US
Actual Output	nXREST nXHOLD reset isys_error CLK320US CLK80US
Pass / Fail Criteria	Pass

If the component test results meet all the functions designed by the SDS, the test is considered to have passed. If any component test results in an error, the test result on that test case is considered a failure. In

addition, the cause of the error is provided to the designer to correct the error of the NLCPU2.

4. Conclusions

In this paper, we designed the test items, test case extraction, test method, test environment, and test procedure for NLCPU2 component test. By comparing the actual results simulated using the testbench with the expected results specified in the software design specification, it was confirmed that the NLCPU2 components were implemented according to the design requirements. The component test results verified the functions of the designed POSAFE-Q processor module PLD logic. In the future, it will optimize the operation of safety-grade PLC by reflecting the results of component test, and an integration test, which is a test to verify whether the interface with other hardware works or not, will be implemented.

REFERENCES

[1] MyeongKyun. Lee, Development and Application of POSAFE-Q PLC Platform, 3rd International Conference on NPP Life Management (PLIM) for Long Term Operations (LTO), Salt Lake City, UT, USA, 2012.
[2] DongIl. Lee, Design of Design of Communication Board for Communication Network of Nuclear Safety Class Control Equipment, JKIICE, Vol. 19, No. 1, pp.185-191, 2015.
[3] IEEE Std 1074, Standard for Developing Software Life Cycle Processes, 2006.
[4] IEEE Std. 1012, Standard for Software Verification and Validation Plans, 1998.
[5] SOOSAN ENS, POSAFE-Q NCPU-2Q PLD Logic Software Design Specification, POSAFE-Q-00102-D310-2