Analysis on Static Noise Margin and Single Event Upset of 10T SRAM for Radiation Tolerance

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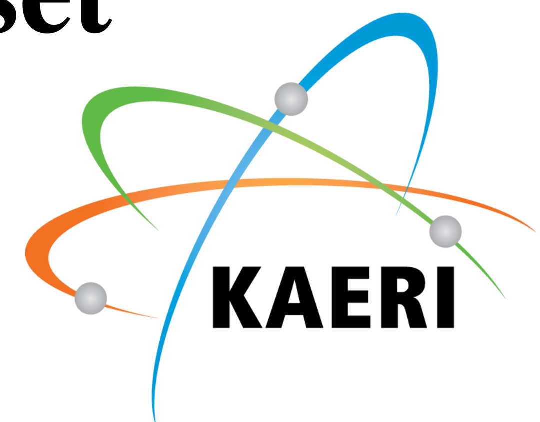
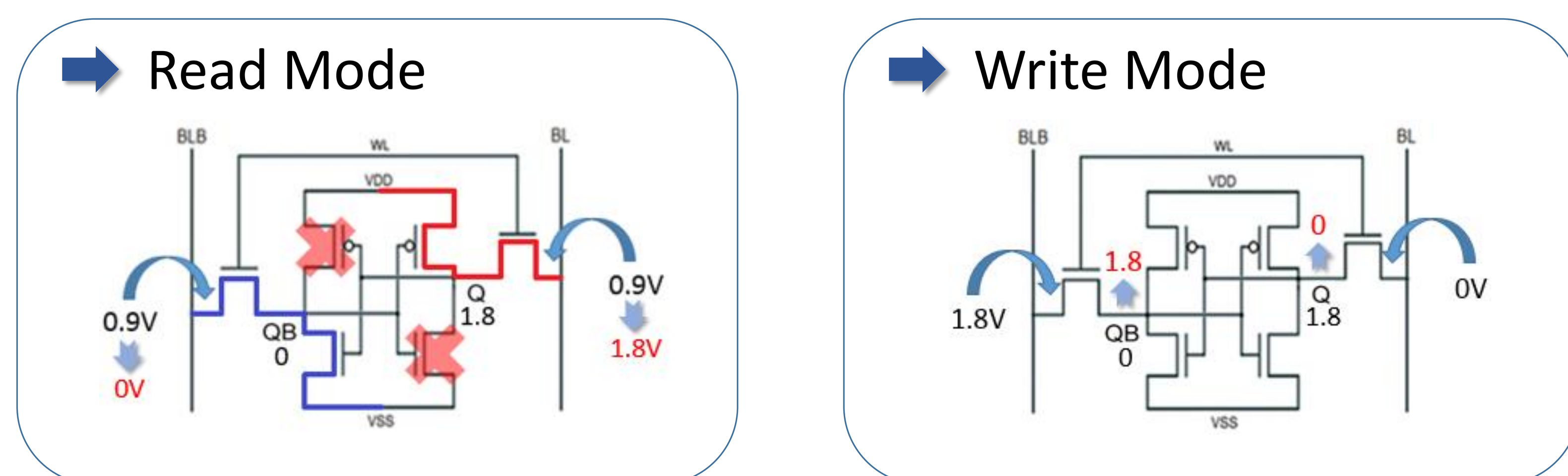


I. Introduction

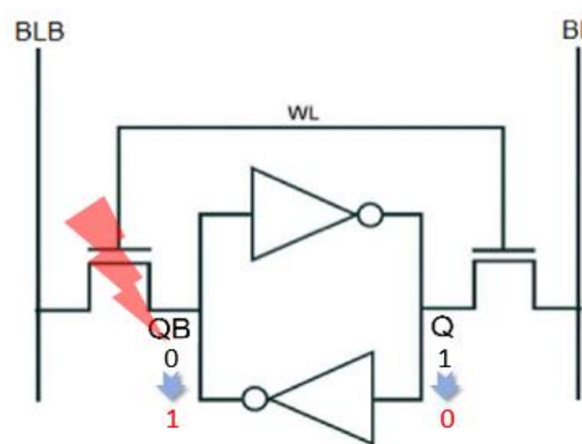
- In the space environment, a common problem in memory semiconductors is soft errors.
- The soft error is a sort of Single Event Effect (SEE) caused by radiation, which means that a single active particle additionally generates electric charges or current inside the semiconductor chip, resulting in malfunction [1].
- SRAMs are vulnerable to radiation, especially when single event upset (SEU) occurs. The SEU is a type of SEE that makes bits inverted [2].
- Proposed 10T SRAM structure has stronger radiation resistance than conventional 6T SRAM in the SEU simulation.

II. Conventional 6T SRAM

- Operation



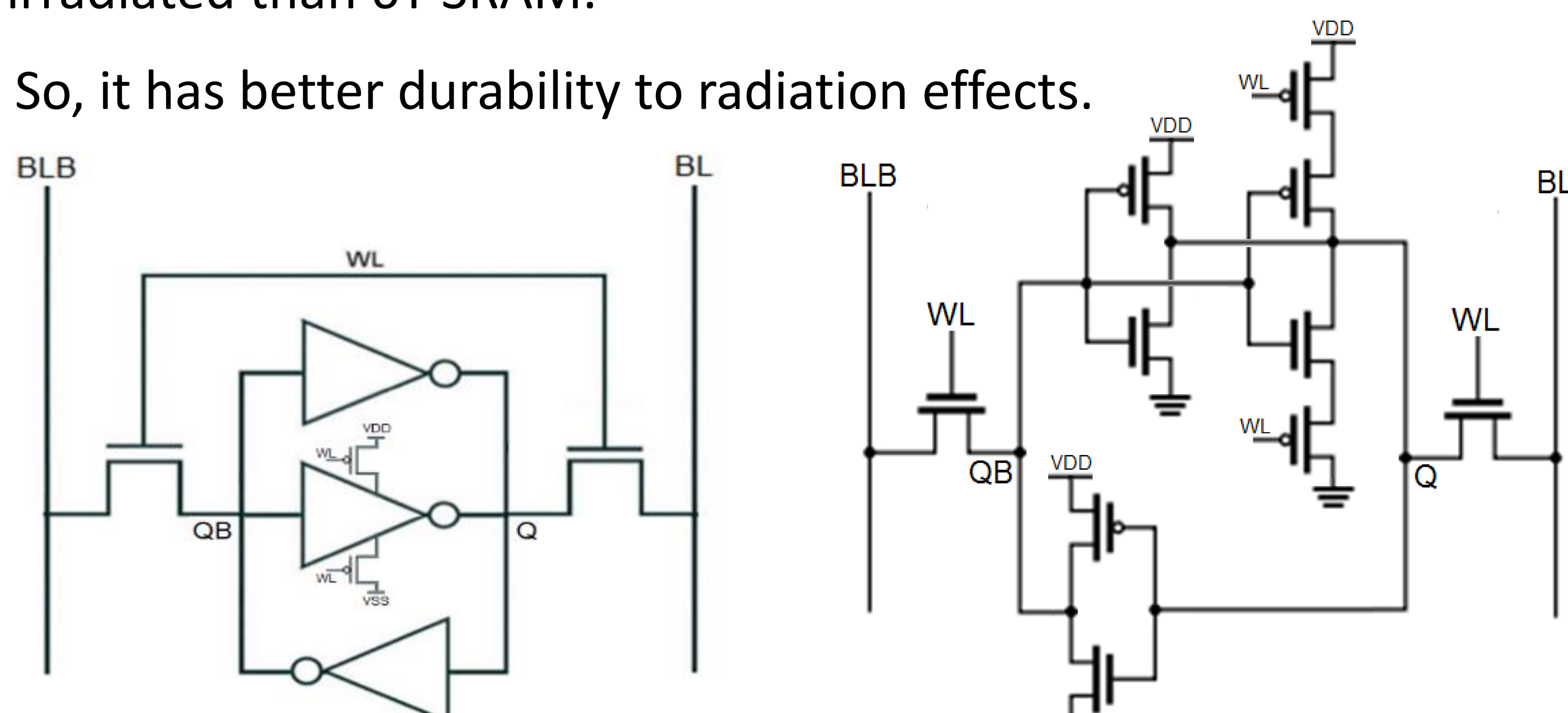
- Single Event Upset (SEU)
  - If the induced current by radiation is injected to these sensitive volumes, the bit of affected node is changed due to the influence of radiation, and then the other is instantly changed along.



  - Therefore, the bit is easily flipped by the radiation in 6T SRAM cell.

III. Proposed 10T SRAM

- Proposed 10T SRAM consists of three inverters in parallel.
- One of them is a tri-state buffer with a PMOS switch at the top and bottom of the inverter, and it raises the drive strength.
- As a result, a 10T SRAM can stand higher radiation energy level after irradiated than 6T SRAM.
- So, it has better durability to radiation effects.

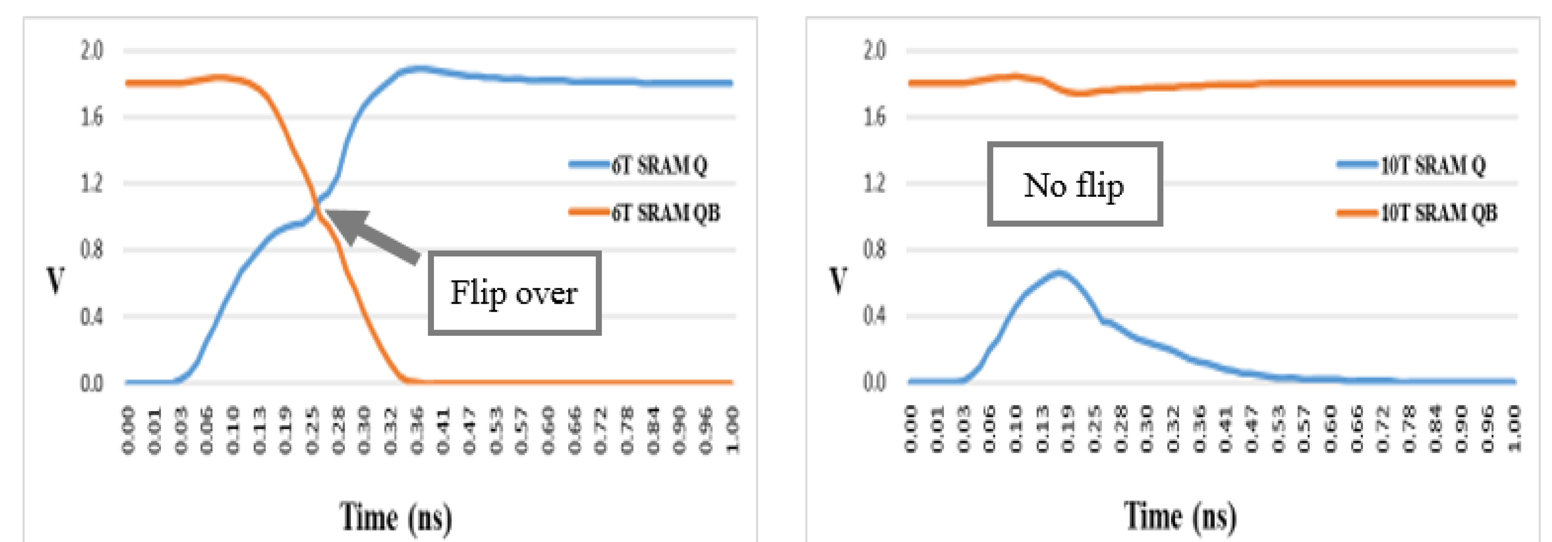


Block diagram of 10T SRAM

Schematic of 10T SRAM

IV. Results

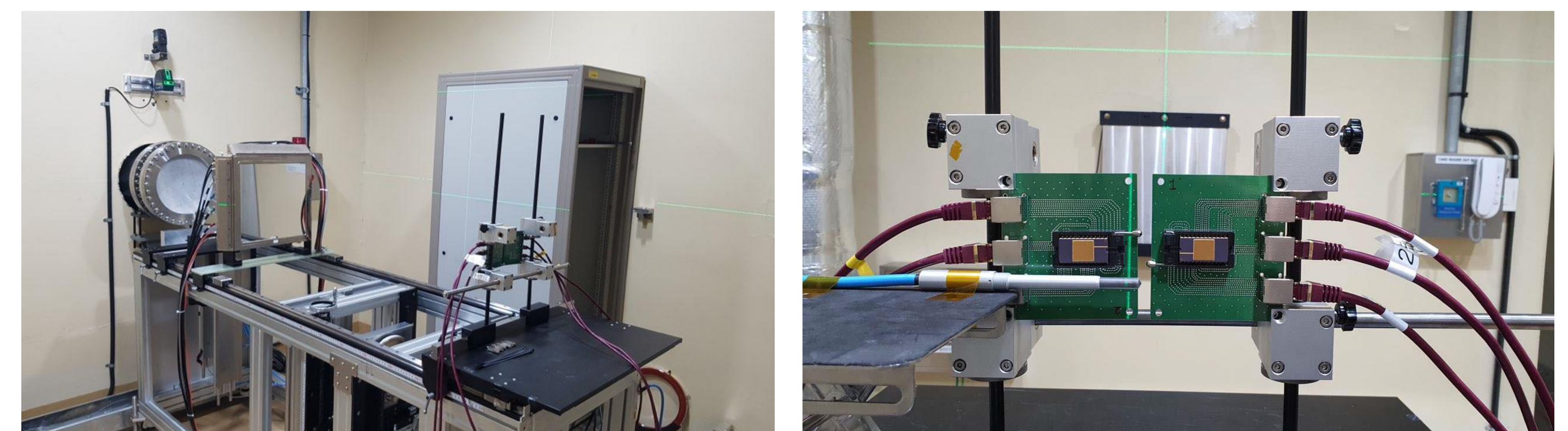
- **Simulation test**
- SEU test of 6T SRAM and 10T SRAM when current is 220 μA.



SRAM	Transistors	Hold SNM	Read SNM	Minimum Current
6T	6	0.716 V	0.316 V	220uA
10T	10	0.7 V	0.316 V	253uA

Table. Comparison of 6T and 10T SRAM

- **Actual irradiation test**
- Radiation test at KAERI KOMAC (Korea Multi-purpose Accelerator Complex)



  - We irradiate the tape-out chip of 6T and 10T SRAM with energy level 69MeV and 100MeV.
  - As a result, there were many soft errors found in the irradiated chips but some issued on data acquisition blocks.
  - The second test will be performed with upgraded SRAM chips this summer.

V. Conclusion

- Conclusion
  - For memory semiconductor devices such as SRAM, soft errors must be considered for harsh radiation environments.
  - So, we design a new 10T SRAM which has an additional tri-state buffer compared to conventional 6T SRAM.
  - Although the hold SNM is reduced by 2.28 %, it does not affect normal operation and LET of the 10T SRAM is 14.8 % better than the conventional 6T SRAM.
  - Result of actual irradiation test on the tape-out chip is not what I expected. And this result shows that there are some effects.
- Future work
  - We have designed the upgraded SRAM chip. And then, the irradiation test will be performed again to obtain the desired results.

Acknowledgement

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References

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