Analysis on Static Noise Margin and Single Event Upset of 10T SRAM for Radiation Tolerance

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1. Introduction

In the space environment, a common problem in memory semiconductors is soft errors. The soft error is a sort of single event effect (SEE) caused by radiation, which means that a single active particle additionally generates electric charges or current inside the semiconductor chip, resulting in malfunction [1].

Static random access memory (SRAM) is now widely used in many digital circuits. The memory device of which cell consists of inverters can retain its stored information as long as power is supplied. Also, it has some advantages in fast processing speed and minimum power consumption. However, SRAMs are also vulnerable to radiation, especially when single event upset (SEU) occurs [2]. The SEU is a type of SEE that makes bits inverted. Therefore, it is critical for SRAM and must be considered when designing for specific applications under radiation environments.

In this study, we propose a new 10T SRAM structure which is simply added a tri-state buffer to a conventional 6T SRAM as shown in Fig. 1 and Fig. 2. The additional tri-state buffer provides more drive strength onto the internal data nodes to prevent a data flip in a situation of SEE. And we compare the performances with the conventional 6T SRAM structure by simulations.

2. Conventional 6T SRAM

2.1 Operation

• Read mode

First, the word line (WL) is given a LOW signal to turn off the access transistors. Then bit line (BL) and bit line bar (BLB) are precharged by half of VDD. When the access transistors are turned on by giving HIGH signal to WL again, the values stored in nodes Q and QB are transmitted into BL and BLB. Finally, it is amplified by a sense amp at the end of BL and BLB.

• Write mode

In contrast to the read operation, the access transistors are initially turned on by applying a HIGH signal to the WL. BL must get HIGH signal for writing HIGH to memory, and LOW signal for writing LOW. Finally, turning off the access transistors by giving the LOW signal to the WL ends the operation and keeps the memory value until next writing.

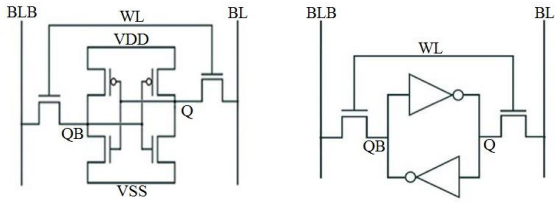

Fig. 1. Schematic and block diagram of the conventional 6T SRAM cell

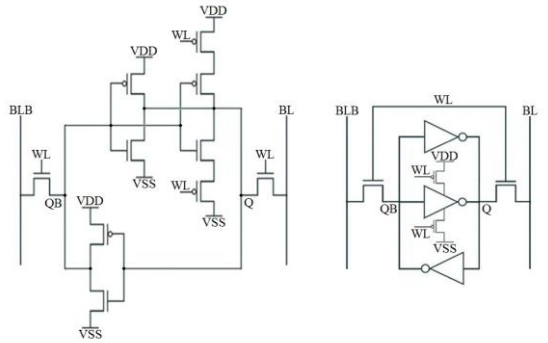

Fig. 2. Schematic and block diagram of the proposed 10T SRAM cell

2.2 Single Event Upset

A data of the conventional 6T SRAM is easily flipped by the radiation. In the worst case, current is generated in a sensitive node due to radiation effects. If the data of the affected node is changed, then the other is instantly changed along. To address this problem, we propose a new radiation hardened SRAM cell using ten transistors.

3. Proposed 10T SRAM

Proposed 10T SRAM consists of three inverters in parallel as shown in Fig. 2. One of them is a tri-state buffer with a PMOS switch at the top and bottom of the inverter, and it raises the drive strength. As a result, a 10T SRAM can stand higher radiation energy level after irradiated than 6T SRAM. So, it has better durability to radiation effects.

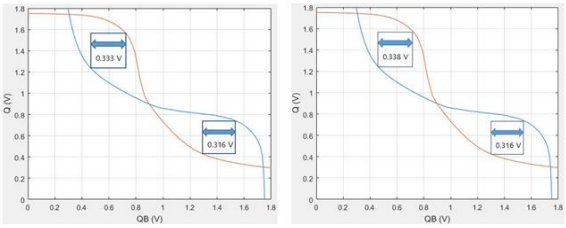

Fig. 3. Read SNM of 6T SRAM (left) and 10T SRAM (right)

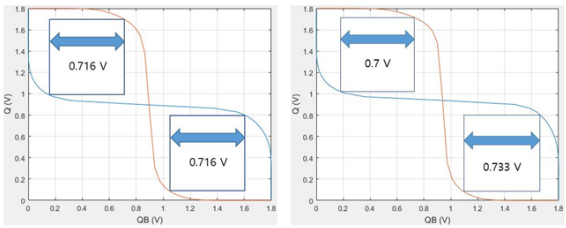

Fig. 4. Hold SNM of 6T SRAM (left) and 10T SRAM (right)

4. Simulation Results

4.1 Static Noise Margin

Static noise margin (SNM) is one of the indicators to determine the stability of SRAM operation [3]. As shown in Fig. 3, read SNM is 0.316 V for both of conventional 6T SRAM and proposed 10T SRAM. But hold SNM of the 10T SRAM is reduced than the 6T SRAM as shown in Fig. 4. However, it does not affect normal operation of SRAM.

4.2 SEU Test Simulation

To verify radiation resistance, we injected the exponential current source to the sensitive node Q or QB in hold mode [4]. As shown in Fig. 5, 6T SRAM data is flipped when 220 µA is injected to the sensitive node Q unlike 253 µA of 10T SRAM. The exponential current source of 220 µA has 43.6 fC and that of 253 µA has 49 fC. Linear energy transfer (LET) can be obtained by: 1 MeV/µm = 4.31 MeV·cm^2/mg = 44 fC/µm [5]. As a result, the proposed 10T SRAM can stand higher radiation energy level of 27.2 MeV·cm^2/mg than the conventional 6T SRAM of 23.7 MeV·cm^2/mg. On actual irradiation tests, we anticipate that a LET value for the bit flip will be obtained much larger because of less leakage current generation induced by radiation than the ideal current source enforcing the node in the simulation.

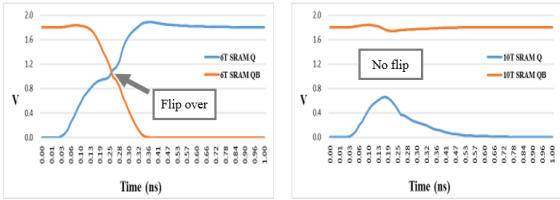

Fig. 5. SEU test of 6T SRAM and 10T SRAM when current is 220 µA.

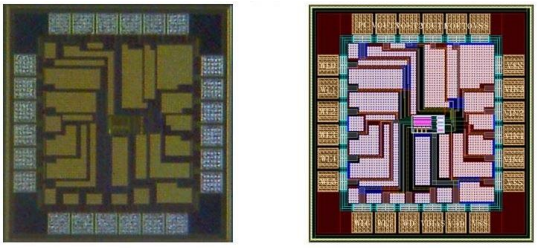

Fig. 6. Proposed 10T SRAM: Test chip photo and Layout

TABLE I
COMPARISON OF 6T SRAM AND 10T SRAM

	6T SRAM	10T SRAM
Cell size (µm^2)	41.69	65.83
Hold SNM (V)	0.716	0.7
Read SNM (V)	0.316	0.316
Cell power consumption (pW)	83.942	97.006
Threshold LET at SEU failure (MeV·cm^2/mg)	23.7	27.2

5. Conclusions

For memory semiconductor devices such as SRAM, soft errors must be considered for harsh radiation environments. So, we design a new 10T SRAM which has an additional tri-state buffer compared to conventional 6T SRAM as shown in Fig. 6. This 10T SRAM cell size is 65.83 µ m^2 and the cell power consumption is 97.006 pW as shown in Table I. The proposed 10T SRAM has SNMs of 0.7 V and 0.316 V and LET of 27.2 MeV· cm^2/mg. Although the hold SNM is reduced by 2.28 %, it does not affect normal operation and LET of the 10T SRAM is 14.8 % better than the conventional 6T SRAM due to the additional tri-state buffer. The simulation results show that the proposed 10T SRAM has better radiation tolerance than the conventional 6T SRAM.

After performing the actual radiation test on the tape-out chip, the results will be announced in conference.

Acknowledgements

This work was supported in part by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (2017M2A8A4017933 and 2020M2A8A1000830).

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