

## Defect Analysis of Schottky Diode based 4H-SiC n-type substrate using Deep Level Transient Spectroscopy

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### 1. Introduction

SiC is a promising semiconductor material which can be utilized in next-generation power device. It has an advantage of high switching speed and low power loss due to its excellent physical properties compared to conventional Si-based devices. On the other hand, neutron transmutation doping (NTD) can be an alternative to mass production of SiC which has a low diffusion coefficient. It is essential to analyze the defects of NTD SiC because it involves various defects caused by neutrons and gamma rays in the research reactor.

In this study the defects of the n-type 4H-SiC substrate was investigated and analyzed by employing DLTS (deep level transient spectroscopy), as a preliminary study.

### 2. Methods and Results

#### 1.1 Sample preparation

N-type 4H-SiC wafers were supplied Crystals Inc. [1] were used to analyze the defect. In order to fabricate SiC Schottky diodes for the measurements, the wafer was diced to 1 cm × 1 cm, followed by a wet etching process. Etching was performed by dipping in TCE (5min), Acetone (5 min), Ethanol (5 min), 20% HF (40 sec) and N<sub>2</sub> drying in turn. Schottky and ohmic contacts were deposited with 100 nm of Ni and Ag, respectively, by sputtering method. Ni was deposited at 1 mm diameter and Ag was deposited overall backside. Figure 1 shows photos of the Schottky and ohmic contacts of the SiC chip.

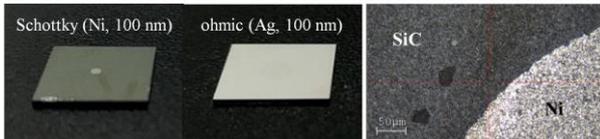


Fig. 1. Fabricated SiC Schottky diode

#### 1.2 I-V and C-V characteristics

I-V and C-V measurements were performed to characterize the Schottky diode. The I-V characteristics at 300K and 78K are shown in Fig. 2. Under the condition of 300K, leakage current was about 20 μA at -2 V. Although the leakage current value was relatively

high, it was determined that DLTS measurement was possible. The C-V characteristics at 300K are shown in Fig. 3. The effective carrier concentration was obtained from the linear regression analysis of 1/C<sup>2</sup>-V plot and the calculated net carrier concentration (N<sub>d</sub>) was 7.73×10<sup>17</sup> cm<sup>-3</sup> which corresponds to about 0.03 Ω·cm of resistivity [2].

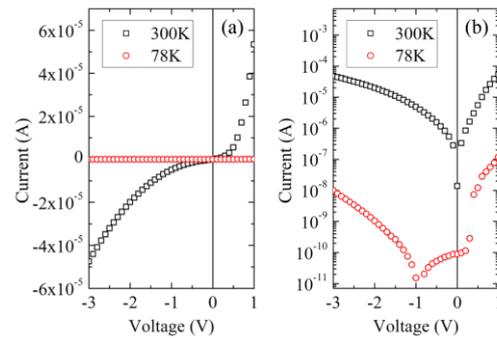


Fig. 2. I-V characteristics of the sample at 300K and 78K in (a) linear and (b) log scale.

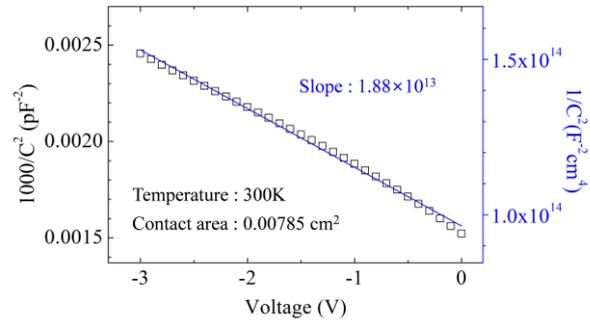


Fig. 3. C-V characteristics of the sample at 300K.

#### 1.3 DLTS measurement

DLTS signal of the sample was obtained using PhysTech FT-1230. The temperature range was 80 to 400K. A reverse bias of 2 V was kept in the measurement. Pulse height and width were 2 V and 0.1 msec, respectively.

Fig. 4(a) shows the DLTS spectrum of the Schottky diode. The spectrum was generally broad, with two peaks (E1 and E2) at high temperature (>300K). The Arrhenius plots of the thermal emission time constants τ (T<sup>2</sup> correction) for E1 and E2 peaks are shown in Fig. 4(b), and the analyzed parameters are shown in Table I.

As shown in the table, two trap levels, E1 (E<sub>C</sub>-0.67

eV) and E2 ( $E_C-1.00$  eV) centers, were observed. Although the sample was an n-type substrate, the energy level of E1 shows good agreement with that of  $Z_{1/2}$  trap which is widely known as an intrinsic defect in 4H-SiC n-type epi-layer [3]. It is understandable because it is considered to be a trap originated from  $V_C$  or  $V_C-V_{Si}$  [4]. E2 seems to be a trap level known as  $RD_{1/2}$  [5]. The origin of the energy level is considered to be  $V_C+V_{Si}$  or  $C_i$ , but it is unclear yet. Furthermore the fact that reported range of the energy is quite wide ( $E_C-0.89$  to  $E_C-1.13$  [5-8]) indicates more accurate identification will be required. Both trap densities are calculated to be about  $3 \times 10^{16} \text{ cm}^{-3}$  which is relatively higher than typical values of 4H-SiC wafer. It seems due to high leakage current of the diode or many defect in the substrate.

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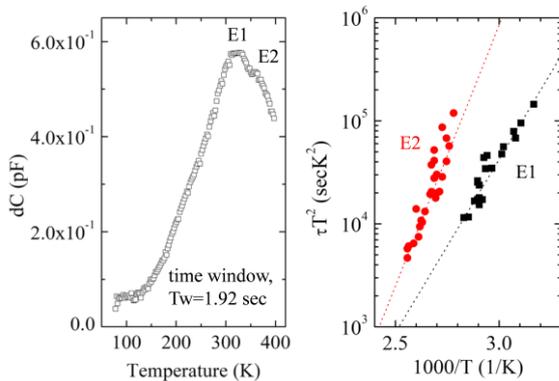


Fig. 4. (a) DLTS spectrum and (b) Arrhenius plots of the sample.

Table I: Trap levels for the sample

Level	Activation energy, $E_a$ (eV)	Trap density, $N_T$ ( $\text{cm}^{-3}$ )	Capture cross section, $\sigma_{\text{eff}}$ ( $\text{cm}^2$ )
E1	0.67	$2.7 \times 10^{16}$	$3 \times 10^{-17}$
E2	1.00	$3.3 \times 10^{16}$	$7 \times 10^{-12}$

### 3. Conclusions

DLTS analysis was performed to evaluate the trap levels in Schottky diode based on 4H-SiC n-type substrate which has  $N_d$  of  $7.73 \times 10^{17} \text{ cm}^{-3}$ . Two defect levels considered as intrinsic defects were observed, and the defect concentrations seems to be highly dependent on the manufacturing process. In future, it is necessary to optimize the electrode structure of Schottky contact in order to increase accuracy of the measurement, considering the detection limit of DLTS system.

### REFERENCES

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