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Design of CMOS Logic Integrated Circuit for Multi-Radiation Environment and Verification of Proton particle and Gamma-ray tolerance characteristics

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1. Introduction

Complementary metal oxide semiconductor (CMOS) electronic devices in radiation environments such as nuclear power plants and space suffer various damages depending on the type of radiation. In particular, total ionizing dose (TID) effect by cumulative radiation (gamma ray, x-ray) and single event effect (SEE) by particle radiation (proton, heavy ion) are dominant [1-4]. In order to develop various radiation-tolerant electronic components in this paper, we analyze the radiation damages of CMOS-based logic integrated circuit (IC), which is an essential element of electronic systems in nuclear power plants and space, and to solve it, silicon on insulator (SOI) and layout modification technologies are applied. The logic chip was designed/manufactured, and its characteristics were verified through the Modeling & Simulation (M&S) and radiation measurement test evaluation.

2. Methods and Results

In this section, the method and results of applying the Geant4-based TCAD tool were presented for virtual simulation of the TID and SEE effects of electronic devices, and a logic chip with a radiation-tolerant structure was fabricated using a 0.8um SOI CMOS process for testing. For the fabricated chip, SEE test results using proton beams of 25 MeV and 55 MeV and TID test results using a Cobalt-60 source up to a cumulative dose of 10 kGy (Si) are presented.

2.1 SEE Modeling and simulation

The SOI process generally forms a buried oxide (BOX) layer on a silicon wafer and is used in high-performance and low-power applications because it has advantages such as high current density and low leakage current compared to the bulk process. In addition, the BOX layer is resistant to single event upset (SEU) and single event latch-up (SEL) phenomena because it can solve the parasitic thyristor turn-on problem caused by the ionization path that occurs when particle radiation passes through the silicon layer [5].

In this paper, in order to predict the SEE tolerance for the SOI process, a 3D characteristic model of a logic inverter and NAND having a general bulk and SOI structure in a CMOS process was designed. SEE simulation by particle radiation was performed for Bulk and SOI logic 3D models [6]. Based on the bulk process structure, simulations were performed according to the angle, position, and energy of the proton particle, and the worst conditions were derived. The greatest damage occurred when proton particles with energy of 25~60 MeV were incident on the source part of the p-type MOSFET in a direction of 90 degrees.

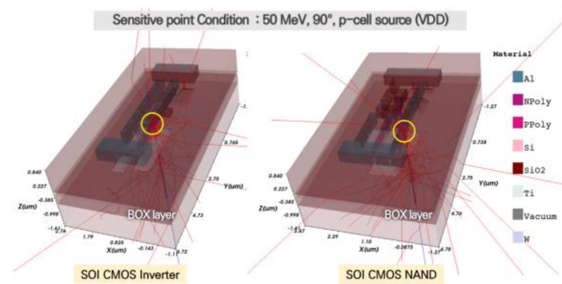


Fig. 1. 3D model of radiation injection of SOI logics including event trace path by 50 MeV proton particle.

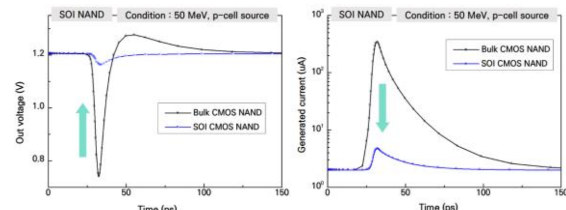


Fig. 2. Simulation result of electrical property change by proton particle (logic high state voltage and its instantaneous current).

Fig. 1 visualizes the event tracking path by 50 MeV proton particles with a 3D logic models of radiation injection. Fig. 2 shows the instantaneous current change of bulk and SOI logic (NAND) due to injected particles under worst case conditions. It was confirmed that SOI logic reduces about 99% in terms of instantaneous generation current compared to bulk logic.

2.2 Rad-hardened Chip Layout Design and Fabrication

Layout design of 0.8um CMOS test process was performed for chip implementation of the SOI logics. In the SOI structure, the BOX layer blocks the SEE effect that occurs instantaneously. However, since ionized charges caused by cumulative radiation are generated in

the oxide region, it is vulnerable to the TID effect. In the end, it adds to the TID effect of the isolation oxide of the general bulk process and causes more damage [7]. In order to mitigate this damage, layout modification design was performed [8]. As shown in Fig. 3, the body contact (+) area is added in the active area (SOI layer) in the general CMOS transistor structure. It is designed to form an empty space and act as a repulsive force to prevent the radiation-induced charges (+) of the isolation oxide layer from affecting the transistor. At this time, Added-gate polysilicon was added to solve the problem of conduction between body (+) and Source&Drain (-). By designing the SOI logics to which this radiation-tolerant layout modification technique was applied, SEE damage was blocked and TID effect mitigation characteristics were secured.

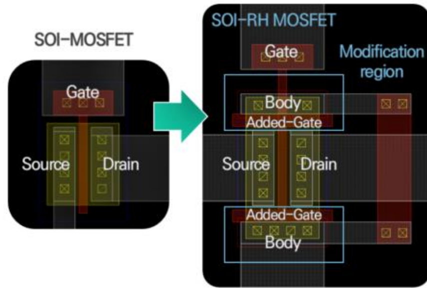


Fig. 3. Drawing of an n-type transistor ball mask with layout transformation technology applied.

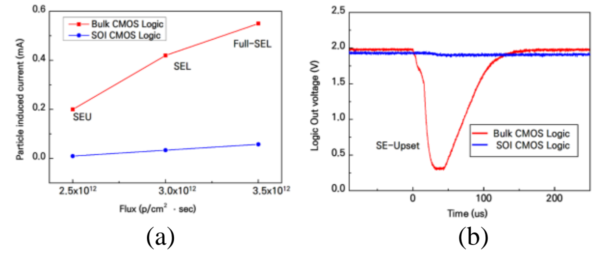
2.3 Radiation Test Results of Proposed Logic chip

Radiation tests were performed on the SEE and TID effects of the manufactured SOI logic, respectively. First, the SEE test was performed [9] with proton beams of 25 MeV (test condition 1) and 55 MeV (test condition 2) at the Advanced Radiation Technology Institute (ARTI) and Korea Multi-purpose Accelerator Complex (KOMAC) in Korea, and each test condition is shown in Table 1.

Table I: Proton beam test condition by facility

Test Facility	Cyclotron (ARTI) condition 1	Linear Accelerators (KOMAC) condition 2
Energy(MeV)	25 MeV	55 MeV
Beam current(uA)	~15uA	0.055 uA
Flux	~5.0×10^{12} protons/cm^2·s	5.0×10^{9} protons/cm^2·s
Dose	~ 3×10^{6} rad(Si)/s	3×10^{3} rad(Si)/s
Beam Pulse width	2 ms (Duty 20%)	50 us
Beam Frequency	1 Hz	1 Hz
Beam spot	13 mm	30 mm

As a result of the SEE test evaluation, in test condition 1, the bulk logic caused SEU and SEL phenomena as shown in Fig. 4 (a) due to the increase in internal instantaneous current due to the increase in flux, while the SOI logic current hardly changed. Even in tset condition 2, compared to the bulk logic in which an upset occurred due to an instantaneous current of about 0.3 uA under the same condition, only a minute current change was observed (Fig. 4 (b)), so the immunity characteristics of the SOI logic against particle radiation were verified.



(a) (b)

Fig. 4. Damage and tolerance characteristics through proton particle radiation tests of SOI and bulk CMOS logic (a) Instantaneous current according to flux increase using ARTI's cyclotron 30 MeV proton beam, (b) Output voltage change at flux of 5.0×10^{9} protons/cm^2·s of 55 MeV proton beam of KOMAC linear accelerator

The TID effect test was performed using the high-energy gamma ray irradiation facility of the ARTI, and the total cumulative dose was irradiated up to 10 kGy (Si) at a dose rate of 5 kGy/h (Si). As a result, as shown in Fig. 6, the SOI CMOS logic was measured to have a higher leakage current change according to the dose increase than the bulk logic. This leakage current amount is a level that can cause malfunction due to performance degradation. On the other hand, the SOI-RH logic to which the radiation-tolerant layout modification technology was applied generated the lowest leakage current. This can be seen as an increase of about 10 times or more in the survival rate of the chip in the cumulative radiation environment.

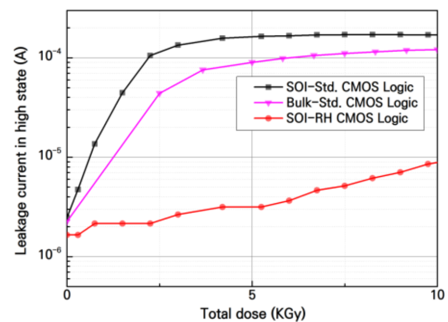


Fig. 4. Measurement result of leakage current change up to cumulative dose 10kGy (Si) of SOI and SOI-RH, bulk CMOS logic.

3. Conclusions

In this paper, we proposed a semiconductor composite tolerance technology that can simultaneously protect the SEE and TID effects caused by particle

radiation and cumulative radiation of CMOS logic. A radiation-tolerant SOI logic chip was designed and manufactured using SOI technology in the process level and layout modification technology in the device level. Through radiation test evaluation, SEE tolerance to proton particles (Table I) and damage reduction characteristics for a cumulative dose of 15 kGy were secured. This result will greatly contribute to the development of electronic systems that are tolerant to radiation that accumulates for a long time in nuclear power plants or space environments and particle radiation that is momentarily incident under special circumstances.

Acknowledgement

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