Development of multipurpose DAQ system using ZYNQ-based digitizer for in 100 MeV Linac and Beam lines at KOMAC

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1. Introduction

In KOMAC, the High Power Radio Frequency (HPRF) system comprises nine Klystrons and the RF system is controlled by digital Low-Level RF (LLRF) control system. The beam diagnostic system comprises devices such as Beam Position Monitor (BPM), Beam Loss Monitor (BLM), Beam Current Monitor (BCM), and wire scanner. Oscilloscopes and high-resolution digital equipment are utilized to measure the RF operation and beam signals. To integrate these measurement devices with the accelerator control system, a distinct interface control system has been developed. To establish a more efficient interface, a new platform has been adopted based on the Zynq chip, enabling easy operation and maintenance, as well as low cost and rapid development. This paper details the development of a Data Acquisition (DAQ) system, based on a Zynq chip and Analog to Digital Converter (ADC), that can be embedded with EPICS Input/Output Controller (IOC) for a large particle accelerator.

2. DAQ configuration

The DAQ system utilizes the AD7606 from Analog Devices, which has eight channels, with four channels used for the DAQ system [1]. The input voltage range is from 0V to 10V, and the resolution is 16 bits, with a LSB (Least Significant Bit) of approximately 0.3mV. The ADC cycle (1-4 channel read) has a minimum time of 1.25us (800KSps), which can be extended as desired, up to 600us. The AC7010 module was used, which contains Xilinx's XC7Z010 Zynq chip to reduce development costs and time for circuit design and artwork [2]. The module has about 100 GPIOs, allowing for the use of external chips, such as the ADC, and does not have extraneous functions like HDMI. The trigger input is used as the ADC data RAM save trigger, and there is a Zynq debug serial port, Ethernet port, and four-channel digital output with TTL output. The TTL output is utilized as a signal for comparing the Voltage Standing Wave Ratio (VSWR) of the forward and pickup signals in the RF waveform, or for comparing the set value of the beam current signal and outputting the result.

3. DAQ system design

3.1 IP Configuration

The Zynq Programmable Logic (PL) is composed of an AD7606 IP for controlling the ADC and I/O, a RAM, an Advanced eXtensible Interface (AXI), and a Zynq processor for the Processing System (PS). Figure 1 shows the IP block diagram. The Top Module for creating the AD7606 IP connects the ADC, RAM, AXI, and AC7010 GPIO for control.

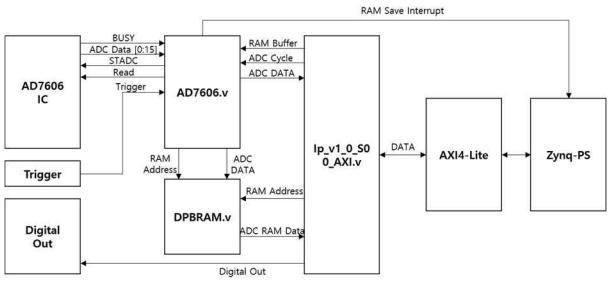
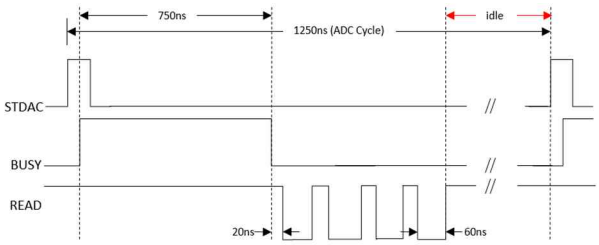


Fig. 1. IP block diagram

The number of ADC data buffers to be stored in RAM and the cycle is only controlled. Figure 2 describes the IP timing diagram on (a) a schematic diagram and (b) a measured timing signals. STADC operates at the set cycle and controls Read and Idle through the Busy signal generated by the AD7606.



(a) Schematic timing diagram

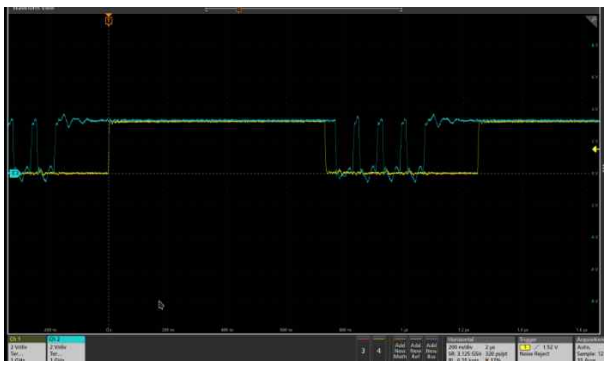


Fig. 2. (b) ADC measured timing signals

If STDAC (ADC Conversion) is set to High, ADC operation commences, and the BUSY signal indicates the progress of ADC conversion, after which the conversion is completed, and BUSY is set to Low. The READ pin is sequentially set to Low to transmit ADC data in 16-bit

parallel format. This process is repeated four times to read all channels, followed by a wait time until the next STDAC signal is set to High. The FPGA sets the ADC's Read signal to Low to read four channels after ADC Conversion is complete, with High and Low set as a minimum of 10ns.

3.2 ADC Data Ram Save

Upon application of an external trigger, the ADC data is stored in the RAM for a set size. This process starts from the next cycle after the trigger is applied, and when all storage is complete, an interrupt is generated as a signal to the PS indicating the completion of the save operation. The Dual Port Memory (DPBRAM) interface assigns Port 0 for ADC data in from AD7606.v and Port 1 for ADC Data Out to PS. The RAM Size is 65536, and both the RAM data width and RAM address width are 16 bits. To configure the RAM for storing ADC data, the ce0 that activates Port 0 is always kept high, and we0 is controlled only when writing to RAM. Port 1 is accessed by the PS through AXI, and data is read by controlling we0 and ce0. An AXI4-Lite interface has been configured to communicate with the PS, and a total of 16 registers have been created, of which 10 are used. The DAQ system has been synthesized using the AD7606 IP, and ports have been established for controlling the ADC and digital out output. The data in the registers communicates with the Zynq-PS area through AXI Interconnect.

3.3 ADC Data Read

With power supply to the DAQ system, the ADC starts operating immediately and is configured to only set the ADC cycle time. Real-time ADC data is continuously updated to the Experimental Physics and Industrial Control System (EPICS) IOC [3]. The Zynq's PL has a dual-port RAM with 65,536 addresses, which can store one ADC data and up to 16,383 data when storing four channels. A high-level application program modifies the size of ADC data to be stored in RAM. ADC cycle time and ADC measurement time are as follows.

$$ADC_{cycleTime} \times RAM_{MaxAddress} = ADC_{MeasureTime}$$

If the ADC cycle time is 1.25μs and 1600 ADCs are stored in RAM, the accelerator driving data collection time is performed for 2ms.

$$1.25\mu s \times 1600 = 2000\mu s = 2ms$$

4. High level application

The EPICS base version R3.14.12.8 is used, and the asyn module is used for AsynPortDriver [4]. waveProc is used for analyzing waveform data from ADC data [5]. Since the Zynq board has an ARM-based CPU, a toolchain is installed for cross-compiling and building programs. When an interrupt occurs in the Zynq PL, the asynPortDriver class definition in the asyn module is referred to for processing I/O interrupt in the PS. When an interrupt occurs, a signal is generated in the kernel module, and the application catches the signal and calls a waveform function to acquire waveform data. The waveform function generates data and then calls a callback function. Data read and write are carried out using the connected pointer through memory mapping with the address connected to AXI.

With the beam accelerator, the beam current was measured, and the data measured in ADC was stored in RAM, and PV was generated by the EPIS IOC waveform record and waveProc record by interrupt. Figure 3 shows the display of measurement data using Control System Studio (CSS).

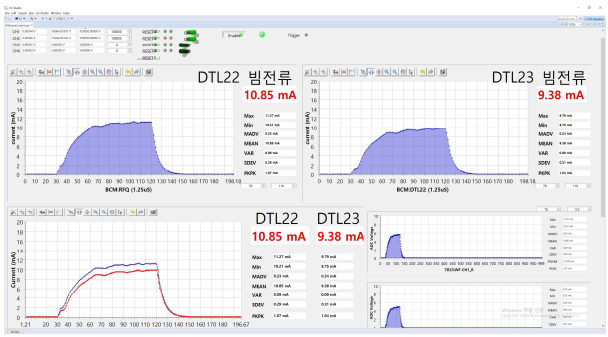


Fig. 3. User interface for beam current monitoring

5. Conclusion

To build a more efficient interface, a new platform based on Zynq chips was adopted, and the design and application development of Zynq chips and ADC hardware was completed. Zynq has Application Processor (AP) and FPGA as on chip, and it is possible to build a compact and low power due to the the advantage of linking CPU and FPGA. The developed DAQ system was capable of low cost and fast development, and stable operation was confirmed in the test. In the future, Zynq-based DAQ system will replace oscilloscopes and high-end digital equipment used to measure beams and RF signals.

Acknowledgement

This work has been supported through KOMAC of KAERI by the Korea government (MSIP).

REFERENCES

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