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Test Results of a Platform for Safety I&C Systems of SMART MMIS

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1. Introduction

SMART (System-integrated Modular Advanced ReacTor), a 330MWt integral pressurized light water reactor that integrates four reactor coolant pumps, one pressurizer, eight steam generators, and one reactor core into a reactor vessel, has been under development at KAERI since 1997. A standard design safety analysis report of the SMART prepared by KAERI was submitted to Korea institute of nuclear safety (KINS) at the end of 2010 [1]. KAERI aims to achieve standard design approval (SDA) from KINS by the end of 2011. SMART MMIS has been designed using digital systems. It has digital-based compact control rooms. Its instrumentation and control (I&C) systems are designed using modular equipment connected through datalinks. Non-safety I&C systems are designed based on the commercial distributed control systems. Safety I&C systems are based on a new platform developed by KAERI. The platform is a high-speed digital signal processor (DSP)-based control unit. It plays the role of a module that provides control functions of the safety I&C systems. The test facilities have been developed at KAERI since 2009 [2]. This paper presents the development and test results of the platform.

2. Development of the Platform

The platform, a 19-inch sub-rack, consists of the following boards, as shown in Fig. 1:

- 300 MHz DSP-based CPU board (CPB)
- 10 Mbps communication board (CMB)
- 8 channel analog input board (AIB)
- 8 channel analog output board (AOB)
- 16 channel contact input board (CIB)
- 16 channel contact output board (COB)
- Sub-rack power module (SPM)

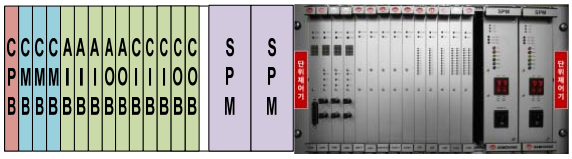

Fig. 1. A typical configuration of the platform

All tasks running in the platform are processed every 25 ms by a cyclic executive scheduler in the following sequence:

- Reset watchdog timer task
- Input processing task
- Logic processing task
- Output processing task
- Self-diagnosis processing task
- Idle

The reactor protection systems (RPS) and engineered safety features component control system (ESF-CCS) run all tasks every 25 ms, but the SMART core protection system (SCOPS) runs all tasks every 50 ms. The processing sequence of all tasks is predetermined and static, and thus it is not changed or preempted. Each sub-rack is independently processed. When a task is stuck or overrun so that the scheduler cannot reset the watchdog timer at the right time, the timer resets the DSP so that the platform stops running and enters a halt state. This feature implies a fail-safe operation of the platform. The CPB provides the following self-diagnosis functions:

- Mirror memory read and write integrity test
- Diagnosis of a mirror memory integrity checker
- Process health check by a watchdog timer
- Diagnosis of a watchdog timer
- A set of instruction operability tests
- Application program integrity test by checksum
- Detection of overflow, underflow, and divided by zero in a calculation
- Detection of stack overflow

The CPB also checks the health of each board in the platform. According to the criticality, the results of the self-diagnosis make the platform enter a halt state or keep operating with warning messages. A 10/100 Mbps communication chip in the CMB is used for full-duplex data transmission between two platforms through separated Rx/Tx ports.

3. Test Results of the Platform

Testing the platform is performed in two steps. Each board in the platform is individually tested in the first step. The interface between two platforms is tested in the second step. In the first step, the CPB, CMB, and I/O boards are tested.

The CPB has the following responsibilities:

- Logical calculation
- Control of I/O boards in the platform

As a test result of the logical calculation, the SCOPS application, which is the most complicated application in the safety I&C systems, was successfully executed within 15 ms. As a test result of the control of the I/O boards, the CPB read 4-byte data from the memory of a board within 1.8 us and wrote 4-byte data to the memory of a board within 3.9 us. The self-diagnosis of the CPB and health-checks of the I/O boards worked properly.

The CMB was tested in a loop-back manner. The CMB transmitted 2442 packets, 512-byte per packet, in 741 ms without error.

Two types of AIBs were tested: 4-20 mA and 0-10 V. Four 16-bit analog-to-digital convertors (ADC) are installed in an AIB. Two types of testing were performed: response time and accuracy. To test the response time, a live signal is input to the AIB through a multi-meter, and a signal from the ADC is captured through an oscilloscope. As a test result of the response time, 95% of the full span of the AIB(4-20 mA) and AIB(0-10 V) was reached in 0.6 ms and 0.7 ms, respectively. In order to measure the accuracy, test results were achieved through more than 100 tests. The error in the mean value of the results was within 0.1% of the full span. The testing was done using a calibrated multi-meter and oscilloscope after adjusting the gain and offset of the AIBs.

Two types of AOBs were tested: 4-20 mA and 0-10 V. A 12-bit digital-to-analog convertor (DAC) is installed in an AOB. Two types of testing were performed: response time and accuracy. To test the response time, a digital signal is input to the AOB from the CPB, and a signal from the AOB is captured through an oscilloscope. The response time is the measured time between the test point in the CPB and output point in the AOB. 95% of the full span of the AOB(4-20 mA) and AOB(0-10 V) was reached in 0.02 ms and 0.06 ms, respectively. In order to measure the accuracy, test results were achieved through more than 100 tests. The error in the mean value of the results was within 0.1% of the full span.

To test the CIB, DC 24 V, 48 V, and 125 V input signals were used. The response time of the CIB showed 3.6 us. To test the COB, the response time is the measured time between the test point in the CPB and output point in the COB. The response time showed 4.8 ms. A relay in the COB delayed the output by about 4 ms.

To test the interface between two platforms, the testing environment was configured as shown in Fig. 2. The code composer studio (CCS) was used to download a test program into the DSP and view the values of the memory in the DSP.

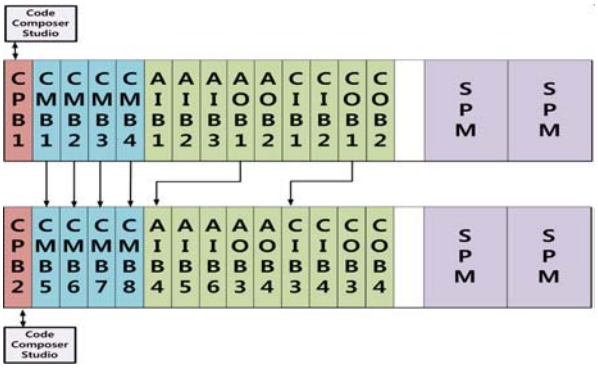

Fig. 2. Platform Interface Testing Environment

The purpose of the interface testing is to check the correctness of the data transmission and response time between two platforms. Two paths were tested: analog signal interface and contact signal interface. The analog signal interface was tested to check the analog signal transmission between two platforms. CPB1 generates digital values for 8 channels, a digital value of 0 V for Ch. 1, 1 V for Ch. 2, 2 V for Ch. 3, 3 V for Ch. 4, 4 V for Ch. 5, 5 V for Ch. 6, 6 V for Ch. 7, and 9 V for Ch. 8, and sends them to AOB1. AOB1 converts them to the corresponding analog signals and sends them to AIB4. AIB4 converts the analog signals received from AOB1 into the corresponding digital values and sends them to CPB2. CPB 1 sends the digital values to CPB2 through CMB1 and CMB4. CPB2 compares the digital values from CPB1 with the converted values from AIB4. The values were correctly transmitted in 0.8 ms.

The contact signal interface was tested to check the contact signal transmission between two platforms. CPB1 generates 16 digital values, 0 or 1, and sends them to the channels 1 through 16 of COB1. COB1 converts them to the corresponding contact signals and sends them to CIB3. CIB3 converts the contact signals received from COB1 to the corresponding digital values and sends them to CPB2. CPB 1 sends the digital data to CPB2 through CMB2 and CMB6. CPB2 compares the data from CPB1 with the data from CIB3. The values are correctly transmitted in 5 ms.

4. Conclusions

A DSP-based high performance platform for SMART MMIS has been under development at KAERI since 2009. The platform plays the role of a control unit for SMART MMIS safety I&C systems. The purpose of testing the platform is to validate the feasibility of the control functions for the safety I&C systems. Based on the test results, the platform satisfied the requirements and specifications imposed on the platform.

The development of a dual CPB will be carried out as a further study.

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