Resource Analysis for Digitalization of FPGA-based Logarithmic Power Signal Processor of ENFMS

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1. Introduction

In the APR1400, the latest Korean nuclear power plant, although most traditional analog instrumentation and control (I&C) systems have been developed as digital systems based on PLCs and DCSs, ENFMS (Ex-core Neutron Flux Monitoring System) still remains an analog system. However, due to concerns over device termination and continuous demands for digitalization, ENFMS also needs to be digitalized.

The PLC based safety grade digital platform, which currently verified and developed at nuclear power plants in Korea, is impossible to process real-time pulse signals in nanosecond units, but ENFMS should process those kind of signals. In order to apply digital technology to ENFMS, new technology development and verification are essential. Currently, a research project is underway for the development of an FPGA-based ENFMS Logarithmic power signal processor, which is the representative signal processor of ENFMS. FPGA was selected in consideration of CCF (Common Cause Failure) and parallel processing capacity for real-time signal processing. In addition, we also referred to reference documents [1], [2] and [3] which show the cases of digitalization attempts using FPGA. Prior to the development using FPGA, a hardware resource analysis should be performed first, and this paper shows the analysis results.

2. Digital ENFMS Hardware Resource Analysis

This section describes the results of analyzing hardware requirements for ADC (Analog to Digital Converter) and FPGA to implement logarithmic power signal processor as a digital system.

2.1. Analyzing ADC Hardware Requirements

[Sampling Rate] ADC, according to Nyquist theory, must sample at a frequency that is at least twice the maximum frequency of the input signal. The input signal of ENEMS is a pulse type signal, and the general shape of the pulse type can be expressed as follows (1).

$$\mathrm{I(t)} = \mathrm{I_0}\left(\mathrm{e^{-t/T_d}} - \mathrm{e^{-t/T_r}}\right) \quad (1)$$

If this is confirmed in the frequency domain, it has an infinite range of frequency components. However, since the sampling rate must be set to a finite value, the Parseval theorem was cited. The Parseval theorem states that the total energy in the time domain is equal to the total energy in the frequency domain. Therefore, the sampling rate should be selected in consideration of some energy loss that will occur during sampling. In this study, the energy loss rate was set to less than 10%. As a result, if the maximum frequency is set to approximately 400MHz, 91.08% of the energy could be preserved compared to the entire range. In this case, the width of the pulse was set to about 100 ns. Finally, according to Nyquist theorem, the sampling rate should be more than 800 MHz, twice 400 MHz.

[Resolution] The height of the pre-amplifier output pulse signal varies from manufacturer to manufacturer, and generally has an output of tens to hundreds of mV. The LSB (Least Significant Bit) value according to input voltage and resolution of ADC can be calculated as follows (2).

$$\mathrm{LSB} = \mathrm{V}_{input} \times \left(\frac{1}{2}\right)^{resolution} \quad (2)$$

If the resolution is set to 10 bits and the input voltage is set to 0~3V range, LSB becomes approximately 2.93mV according to equation (2). If the resolution is 10 bits or more, it is expected that it will be sufficient to distinguish neutron signals from gamma signals because the neutron signals are normally more than twice as large as the gamma signals. Accordingly, we set the minimum requirement for resolution to 10 bits. However, since it is not a result from all the functions of logarithmic power signal processor but a result from a kind of function, the resolution should be complemented according to the results of performance analysis in the future.

The table 1 shows some commercial ADCs with a sampling rate of 800MHz or higher and resolution performance of 10bit or higher.

Table 1. Examples of commercial ADCs that satisfy the performance

Model No.	Resolution	Sampling rate
AD9217BBPZ-6G	12 bit	6 GHz
AD9083BBCZ-RL7	16 bit	1 GHz
AD9209BBPZ-4G	32 bit	4 GHz

2.2 Analyzing FPGA Hardware Requirements

Figure 1 shows the functional components of signal processing of logarithmic power signals (representative signals) to be composed of FPGA.

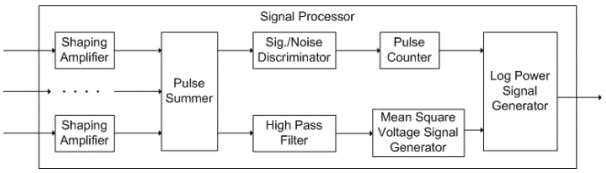

Figure 1. Signal processing diagram for logarithmic power signal

Resource analysis necessary for implementing FPGA hardware was performed based on the algorithms of each of the above components established for digital signal processing in reference documents [4] and [5]. For the analysis, IP (Intellectual Property) provided by Xilinx Vivado was used, and the Resource analysis tool was used.

Figure 2 shows an example of analyzing hardware resources using the tool provided by Xilinx. The logarithm unit shown in the example is one of the components of the Log Power Signal Generator shown in Figure 1.

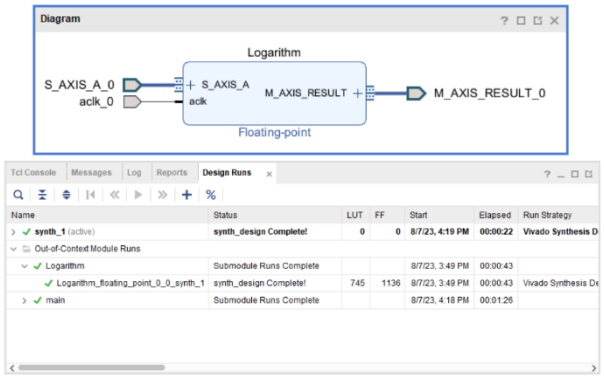

Figure 2. Hardware resource for logarithm function block

The analysis results for each component and overall hardware resources for logarithmic power signal processor in Figure 1 are summarized in Table 2. In summary, a FPGA chip with more than 45,128 logic cells and more than 3,896 flip-flops is required.

Table 2. Hardware resource analysis results required for implementation using FPGA

Component	Logic cells	Flip-Flops
Shaping Amplifier	11,241	288
Pulse Summer	96	-
Signal/Noise Discriminator	36	-
Pulse Counter	1,249	32
High Pass Filter	27,494	-
Mean Square Voltage Signal Generator	2,254	64
Log Power Signal Generator	2,758	3,512
Total	45,128	3,896

And Table 3 shows Xilinx FPGA products that meet the hardware resource requirements analyzed above.

Table 3. Examples of commercial FPGA chips that satisfy the performance

Model No.	Logic cells	Flip-Flops
Artix-7 XC7A50T	52,160	65,200
Artix-7 XC7A75T	75,520	94,400
Kintex-7 XC7K160T	25,350	162,240
Kintex-7 XC7K325T	50,950	326,080
VITEX-7 XC7V585T	582,720	728,400
VITEX-7 XC7VX330T	356,400	408,000
Kintex UltraScale AU10P	96,000	88,000
Kintex UltraScale AU15P	170,000	156,000

3. Conclusion

This paper shows the results of analyzing the necessary resource of ADC and FPGA chip required to implement the logarithmic power processor. As a result of evaluation, this paper confirmed that implementing a FPGA-based logarithmic power signal processor is feasible. This time, a resource analysis for a part of ENFMS was performed, but in the future an optimization analysis of the entire ENFMS system should be performed.

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