Development of RF Monitoring System using EPICS for KOMAC Linac

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1. Introduction

The 100 MeV linear accelerator (Linac) has been successfully operated for over a decade at Korea Multi-purpose Accelerator Complex (KOMAC). The control system is implemented based on a distributed control system Experimental Physics and Industrial Control System (EPICS) which can organically link and control various accelerator components. Recently, new ADC device was developed that the Zynq SoC based ADC [1]. This ADC device can not only visually show signals from the accelerator without an oscilloscope, but also enable real-time data processing without any additional device. In this paper, the Zynq SoC-based ADC for RF power monitoring is presented. The goal is to upgrade the EPICS IOC for data processing of ADC and Zynq. The development of RF monitoring system will be applied for stability of the accelerator.

2. RF control system

The 100 MeV Linac at KOMAC typically consists of a microwave ion source, RFQ, DTL, and various accelerator components. To operate and extract proton beams, an RF source is supplied at 350 MHz. RF directly affect acceleration and focus the proton beams inside the DTL, therefore RF control system is essential to provide high quality proton beams. For the 100MeV linac, 11 LLRF control systems have been operated with RF digital feedback control system as shown in Fig. 1.

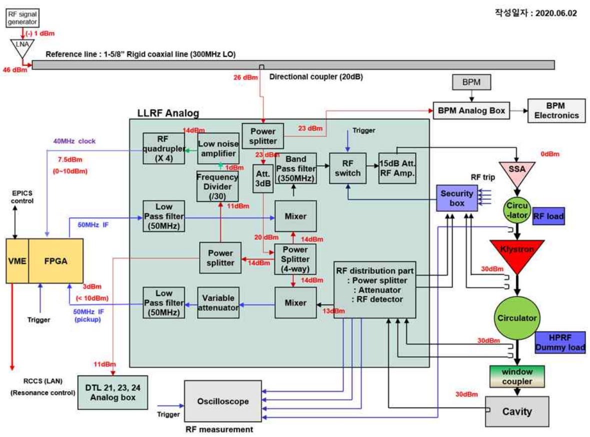

Fig. 1. Schematic layout of the digital and analog system for LLRF control system

The LLRF control system is composed of the Emerson MVME5100 board as a baseboard and the PENTEK 7142 FPGA PMC extended board for implementing feedback control logic, including several digitizers, such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

As shown in Figure 1, the cavity pickup signal is input to the LLRF system for RF feedback control. And the rest of the driving signals are monitored using an oscilloscope. Here, an ADC-based DAQ system is developed to monitor and analyze RF operation signals.

3. DAQ RF monitoring system

As hardware for RF monitor, Digilent zybo-z7-20 and Analog Device AD7605 ADC are adopted [2]. A development environment is established with Vivado Design Suite and Petalinux for the development of ADC devices and EPICS IOC servers on Zynq SoC. Fig. 2 shows the configuration of the Zynq SoC based ADC.

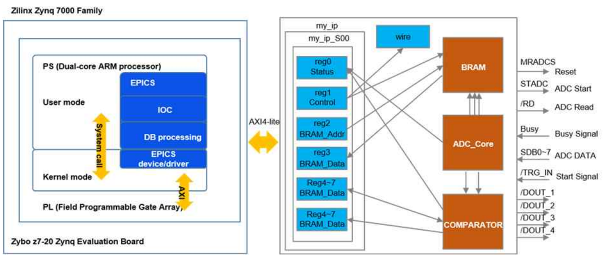

Fig. 2. Configuration of Zynq SoC based ADC and upgrade strategy.

The Zynq uses an AXI interface between PS and PL. on the PL side, there are AXI Master (High Performance) ports, AXI General Purpose (GP) ports, AXI Slaves GP, and AXI Master ACP ports. The PS connected to the PL uses a GPIO controller. The Petalinux tools offers everything necessary to customize, build and deploy Embedded Linux solution on Xilinx processing systems. We customize the boot loader, linux kernel, linux application.

3.1 Establishment of development environment

To check the RF state, RF power is monitored through EPICS IOC [3]. This converts the RF voltage signal measured from the oscilloscope into RF power through an EPICS subroutine record.

And it represents the upgrade strategy of the Zynq SoC based ADC in Fig. 3, which converts the SSA, Forward, and Reverse RF signals input to the ADC channels into their respective RF powers. The function to convert RF voltage signals input to the ADC into RF power will be implemented by including it in the subroutine record. To calculate the RF power, the mean value of the RF voltage signal measured by the ADC is applied. In the EPICS IOC, the function is implemented to simultaneously change the RF power every time the mean value of the RF voltage signal measured by the ADC changes. In addition, the IOC is configured with PVs that can indicate the RF power.

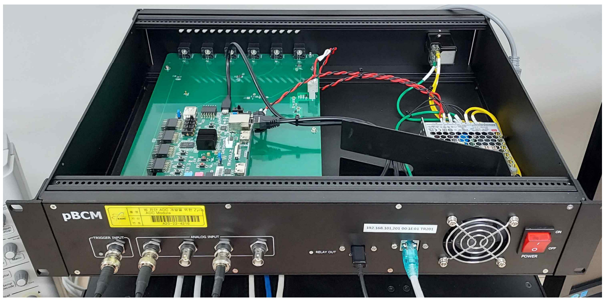

Fig. 3. Test bench for the upgraded Zynq SoC based ADC.

3.2 Local test of RF monitor system

It consists of an upgraded with involved RF power monitoring functionality Zynq SoC based ADC, a waveform generator (WF1974, NF corporation, Japan), and a pulse/delay generator (Model 575, BNC, USA). The trigger for the ADC operation is applied through the pulse/delay generator. During the input of the trigger, the voltage signal values of each channel are sampled by the ADC and the data processing is performed. The appropriate voltage for each channel is input through the waveform generator, and the ADC monitors the RF power by connecting to a PC via a LAN port.

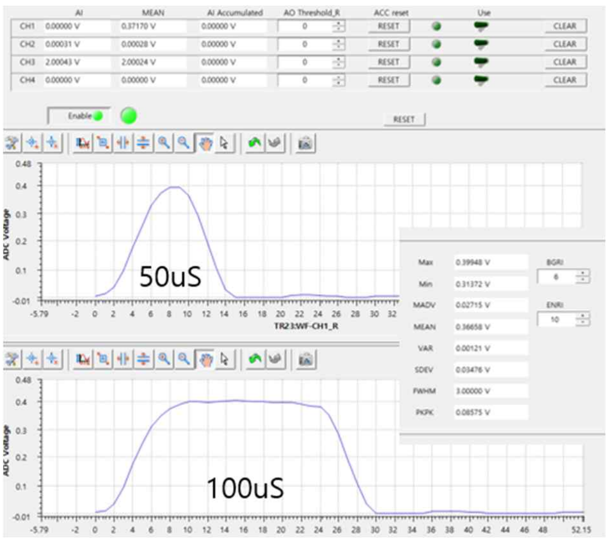

Fig. 4. Waveform acquisition test of RF power monitoring by using CS-Studio.

To monitor and visualize the RF power, CS-Studio was used, which is shown in Fig. 4. At the top of the screen, the ADC signal and RF power value input to the channel are displayed, which can be operated by turning the 'ENABLE button' on/off.

The EPICS IOC operates normally without any problem, and the PV for RF power calculation also appeared. To demonstrate the RF power for the input values in each channel, DC 700 mV signal was input using a signal generator, and a trigger with a pulse width of 10 µs was set for operation. The results show that the RF power values are successfully converted for an input voltage of 700 mV, and there are stable within a deviation of ±0.1 kW, as shown in Fig. 5. In the left site Fig. 5, it shows the voltage input to the ADC and the corresponding RF power is shown on the right site. The RF power graph shows the RF power for each SSA, Forward, and Reverse in order from top to bottom.

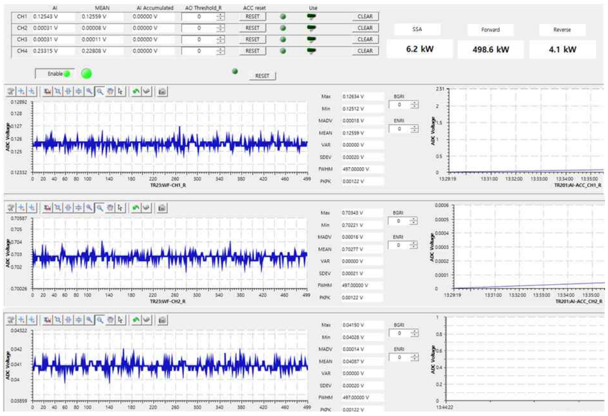

Fig. 5. Results of RF power output with respect to ADC input voltage (Enable state)

4. Conclusion

In this study, the development of the RF monitor system was completed, and the test results confirmed the same value as the existing RF operation data. In the future, DAQ systmes will replace oscilloscopes, and real-time data acquisition and analysis are expected.

Acknowledgement

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