Controller Upgrade for High Voltage Converter Modulator at KOMAC

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1. Introduction

For operating a 100 MeV proton linear accelerator in Korea Multi-purpose Accelerator Complex (KOMAC) of Korea Atomic Energy Research Institute (KAERI), the High Voltage Converter Modulator (HVCM) has been used as a pulse power supply to drive two or three klystrons since 2013. In KOMAC, four HVCMs drive nine klystrons, which supply RF power to the RFQ cavity and DTL tanks. The specifications of a HVCM driving two klystrons are shown in Table I.

Table I: Specifications [1]

Peak Power	5.25 MW
Pulse width	1.5 ms
Max. Repetition rate	60 Hz
Duty	9%
Input voltage to SCR	3.3 kV_{ac}
Max. output voltage from SCR	2.2 kV_{dc}
Flat-top output voltage	105 kV
Flat-top output current	50 A

This type of modulator has an advantage to generate the long pulse width output power. KOMAC modulator can drive the klystrons up to 1.5 ms with less than 1% voltage droop.

The major component of the HVCM is main controller because the controller drives the Insulated Gate Bipolar Transistors (IGBTs) and protects the components with fast interlock system. Also, controller can compensate the flat-top voltage drop less than 1% using a frequency sweep technique.

For handling the obsolete issue of controller components especially logic devices, the necessity of developing new controller was raised up. With this chance, the controller upgrade was also carried out to strengthen the components interlock.

In this paper, we introduce the upgrade contents and results of HVCM controller.

2. Controller upgrades

2.1 FPGA based logic development

The original control system has two types of logic device. The Field Programmable Gate Array (FPGA) was used for interlock summing and Complex Programmable Logic Device (CPLD) was used for IGBTs gating. However, new controller logic device consolidated the IGBTs driving and interlock summing functions in the Lattice MachXO FPGA. Most of algorithm were derived from original design and implemented using VHSIC Hardware Description Language (VHDL).

The pulse flattening using frequency sweep technique also translated from CPLD logic to FPGA logic through VHDL code. As shown in Fig. 1, the frequency sweep operation was verified by test. The IGBT switching frequency varies from 18.587 kHz to 19.379 kHz in 8 steps corresponding to the output current integral signal. Orange trend of Fig. 1 shows the current integral signal by RC integrator and the digital signals (8ch) shown in Fig. 1 describe the frequency changing flag signal.

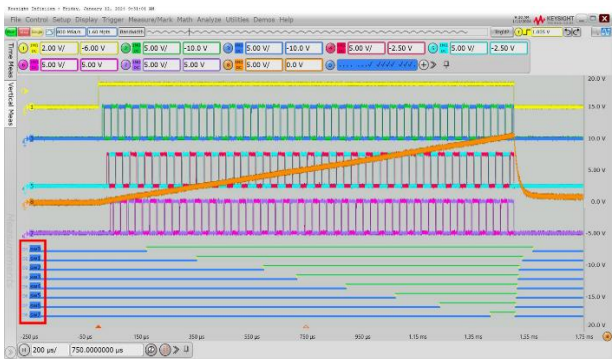

Fig. 1. Waveforms of IGBT drive signals, current integral signal (orange) and frequency changing flag signals (digital).

2.2 IGBT shoot-through protection

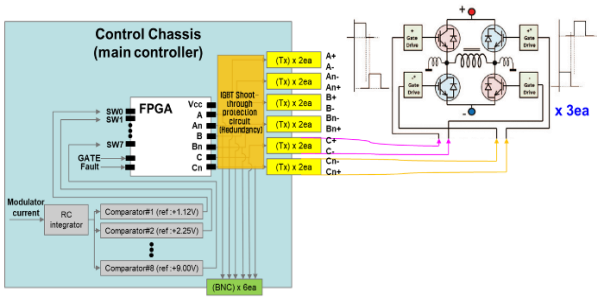

Fig. 2. Block diagram of IGBT gating and shoot-through protection integrated circuit.

In Fig. 2, four IGBTs illustrated in the H-bridge type full bridge inverter. The FPGA in main controller drives the IGBTs simultaneously on diagonal pair. In original

control system, there is no shoot-through protection circuit that IGBTs in inverter have a risk to blast.

To protect the IGBT components in new control system, additional shoot-through protection circuit is built in subsequent FPGA stage. The primary components in Fig. 3 are Gallium Nitride (GaN) FET drivers (Texas Instruments, UCC27611) with a fast (less than 20 ns) switching characteristic. The overlap signal is blocked by the opposite pair active signal on this GaN driver's inverting port. Additionally, the FPGA will receive notification from the coincidence flag signal via SR latch that the HVCM can safely halt the powering system if the coincidence of IGBT drive signals is observed in the Fig. 3 circuit.

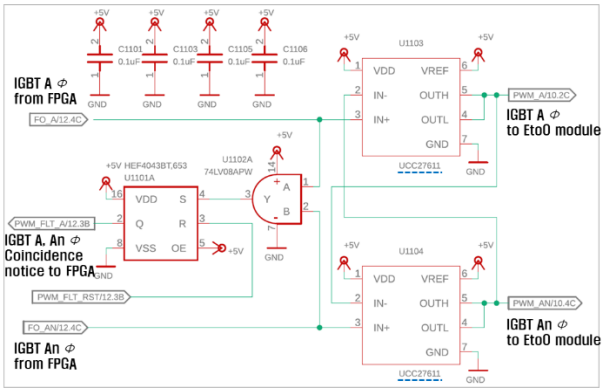

Fig. 3. Schematic of IGBT shoot-through protection circuit.

2.3 Fault waveform capturing

The controller of HVCM monitors the pulsed type waveforms including IGBT drive signals, transformer primary current signals, output voltage signal, output current signal and external gate signal. All signals are monitored through the oscilloscope with external trigger mode. The original control system uses external gate signal coming from timing system as an external trigger. Because of that reason, the waveforms on an oscilloscope disappear even if the HVCM experienced the system trouble.

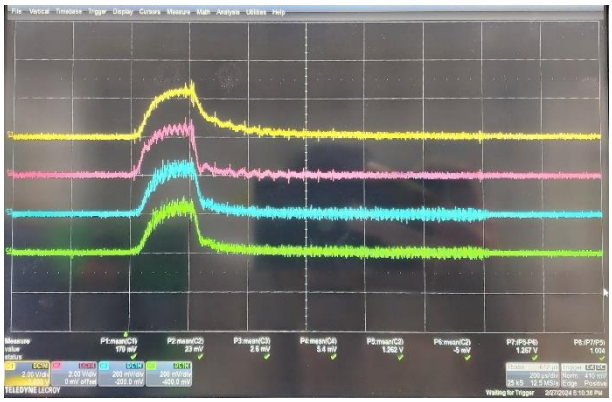
Fig. 4. Captured waveforms at the time of fault detection.

To capture the waveforms in new control system, the controller generates the additional trigger signal synchronized with the external gate signal. This new trigger is linked with the fault flag signal that the oscilloscope can capture the waveforms by stopping the triggering. As shown in Fig. 4, HVCM operation waveforms are latched on the oscilloscope when the output over-voltage fault was detected by a comparator circuit.

2.4 IGBT gate stop condition enhancement

In original control system, IGBT gate signal was stopped only when IGBT experienced the IGBT over-current fault. However, the necessity of reinforcement for IGBT gate stopping condition is increased from operational experience with HVCMs.

As a result, IGBT gate stopping conditions were improved in new controller through FPGA logic upgrade. IGBT gate stop conditions included not only IGBT over-current fault but also conditions related to gate abnormality, output over-voltage, output over-current, IGBT gate coincidence fault, klystron fault and human safety.

3. Test results

Before activating the HVCM, all interlock test for stopping the HVCM was carried out based on the internal procedures. After confirming the interlock system, we check the IGBT gate signal's soundness with long-term. Finally, we energized the HVCM with new controller for testing the single shot pulsing.

3.1 IGBT gate signal long-term test

IGBT driver output is +15 V to -15 V and switching frequency is dependent to the new controller's IGBT gate output signal. IGBT driver output signals were observed through oscilloscope without energizing the HVCM as shown in Fig. 5.

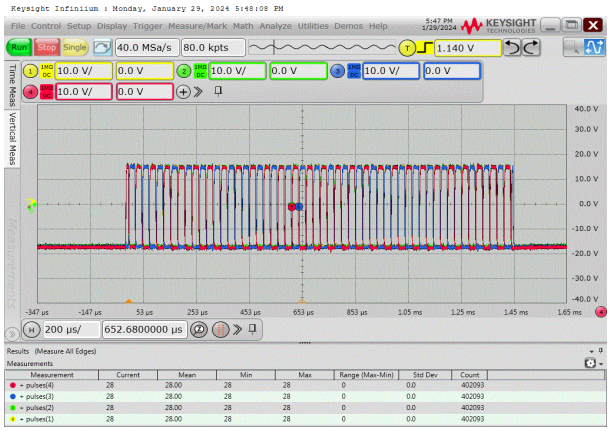

Fig. 5. IGBT driver output signal statistics in oscilloscope.

We verified the switching frequency with long-term monitoring and checked soundness of square waves by using a pulse counting statistics function in oscilloscope.

Quality of new controller output was verified through testing of more than 400,000 shot pulses.

3.2 Single shot test

HVCM was energized for single shot powering. The test goal is reaching the operation value of HVCM using new controller in comparison with original controller.

As shown in Fig. 6, the single shot test pulse width is 1.5 ms and output pulse power attains -95.6 kV, 47.6 A.

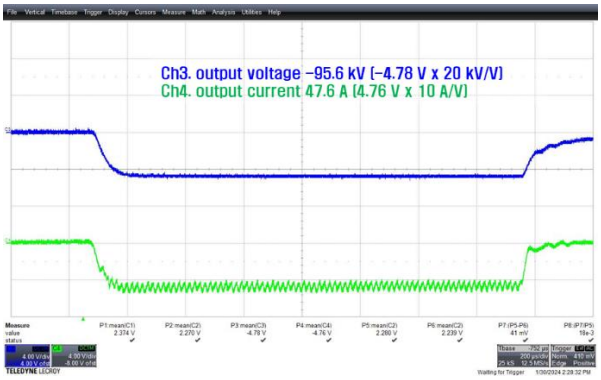

Fig. 6. Single shot test result.

This result satisfies the test goal accomplishing the original operation values.

4. Conclusions

In new controller of HVCM, the FPGA based logic device upgrade was implemented and verified. Through IGBT shoot-through protection circuit, the interlock system reinforced the switching component's life. Also, it is expected that troubleshooting time will be reduced through the fault waveform capturing function. The operational HVCM will be upgraded with new controller by next year.

ACKNOWLEDGMENT

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[1] W. A. Reass et al., "Operations of polyphase resonant converter-modulators at the Korean Atomic Energy Research Institute," in *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 18, no. 4, pp. 1104-1110, August 2011