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# High Speed Active Quenching for Single-Photon Avalanche Diodes Using Digital Radiation Detection

Sundo Kim[a], Jinseok Oh[b], Dongsuk Jeon[a*], and Inyong Kwon[c*]

[a] *Graduate School of Convergence Science and Technology, Seoul National University, 2nd floor, 18-dong, Gwanak-ro 1, Gwanak-gu, Seoul 08826, Korea*

[b] *Korea Atomic Energy Research Institute, 111, Daedeok-daero 989 Beon-gil, Yuseong-gu, Daejeon 34057, Korea*

[c] *Department of Radiological Science, Yonsei University, Wonju, 26493, Republic of Korea*

**Corresponding author: djeon1@snu.ac.kr, ikwon@yonsei.ac.kr*

*E-mail: ksundo@snu.ac.kr*

## I. Introduction

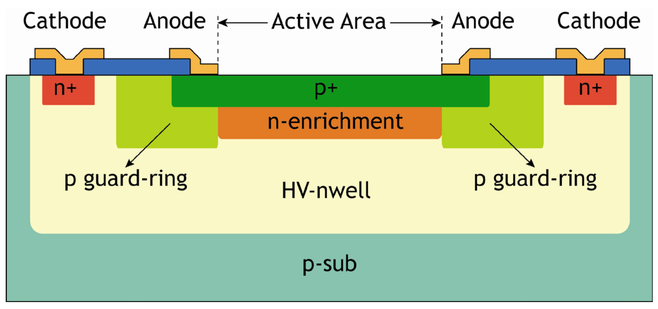


Fig. 1. A common SPAD structure.

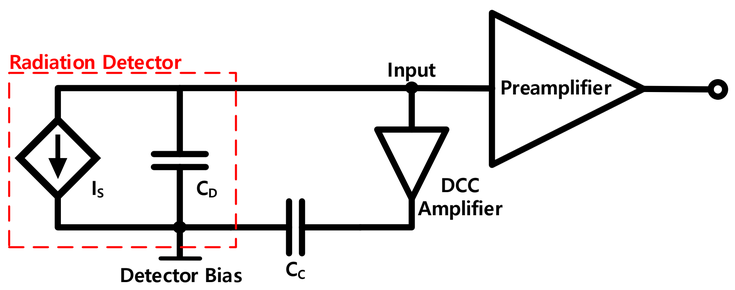


Fig. 2. Configuration with a charge-sensitive preamplifier and a DCC amplifier to compensate the detector capacitance.

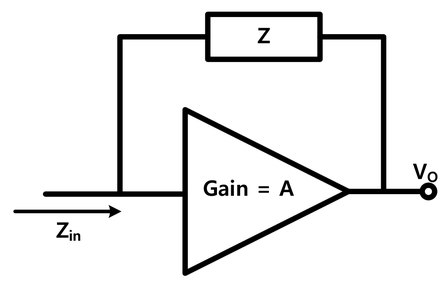


Fig. 3. Circuit diagram demonstrating how the Miller effect is applied to the DCC amplifier in order to seemingly have zero detector capacitance for the downstream readout circuits.

- Single-photon avalanche diode (SPAD) is a photodetector which is a common p-n junction operating when biased above breakdown voltage $V_{BD}$.
- SPAD requires a quenching circuit, small-size and fast response, to cease avalanche operation and recharge to get ready for the next operation.
- Like other photodetectors, SPAD has a larger detector capacitance that deteriorates slewing performance – using detector capacitance compensation (DCC) technique, this deteriorating effect of detector capacitance can be mitigated by means of Miller effect.

## II. Circuit Implementation

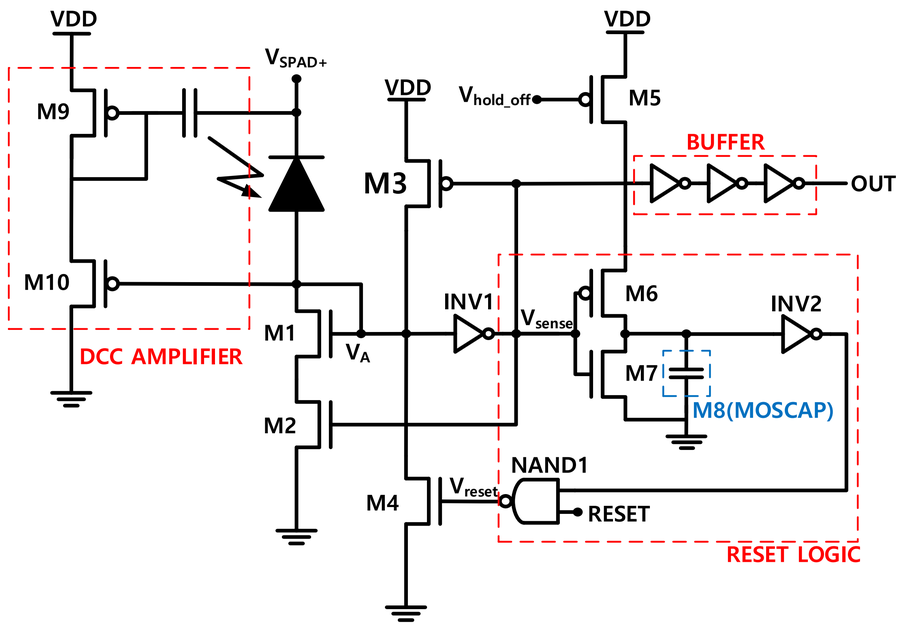


Fig. 4. Full architecture of the proposed design.

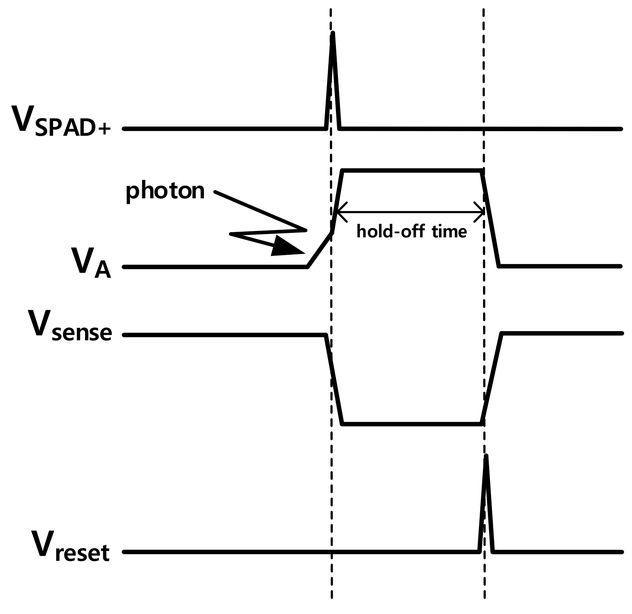


Fig. 5. Timing diagram of basic quenching operation.

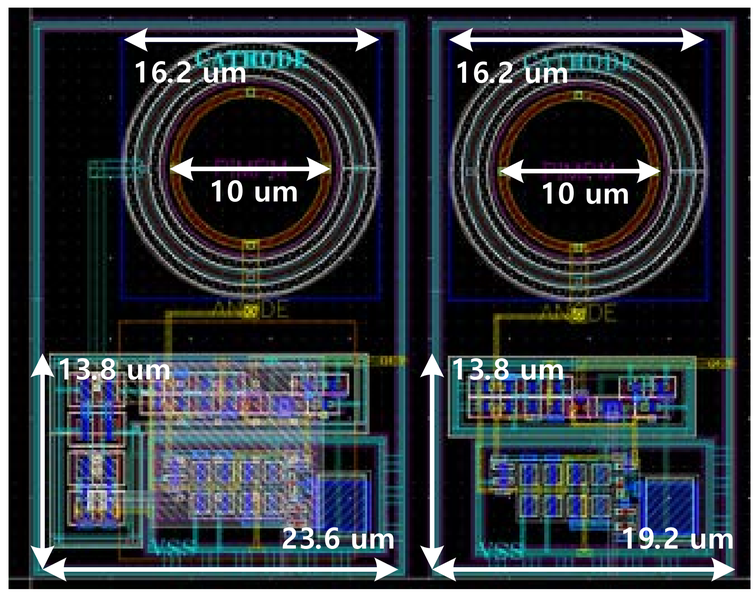


Fig. 6. Layout (Left: proposed, right: conventional)

- Fig. 4 shows the block diagram of the proposed detector compensation technique used in this circuit.
  - DCC amplifier is implemented only using two PMOS transistors and a metal-insulator-metal (MIM) capacitor
  - The hold-off time can be controlled by current-starved inverter
- Fig. 5 shows the timing diagram of basic quenching operation – the DCC technique enhances quenching performance by quick pull up of $V_A$ node up to half VDD.
- MIM capacitor occupies top metal (5 and 6), enabling it to be laid on top of circuit (Fig. 6)
- The proposed active quenching technique shows only 23% area increase compared to the conventional design.

## III. Simulation and Measurement Results

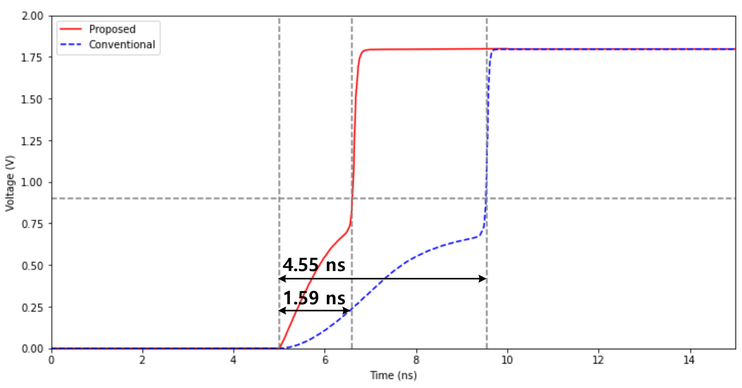


Fig. 7. Simulation results of active quenching at node $V_A$ (Red solid: proposed, Blue dashed: conventional).

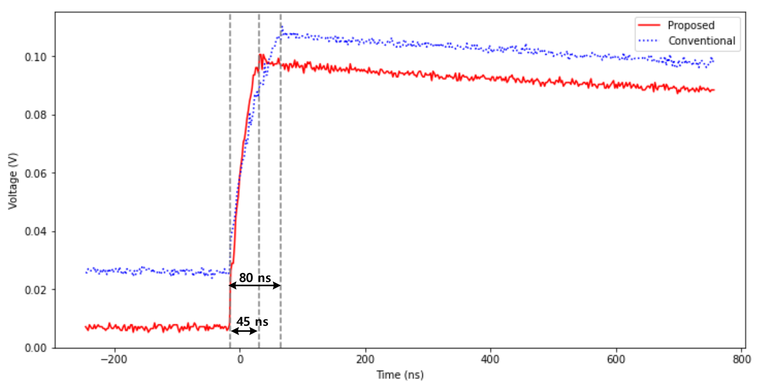


Fig. 8. Measurement results of passive quenching at the anode (Red solid: proposed, Blue dotted: conventional).

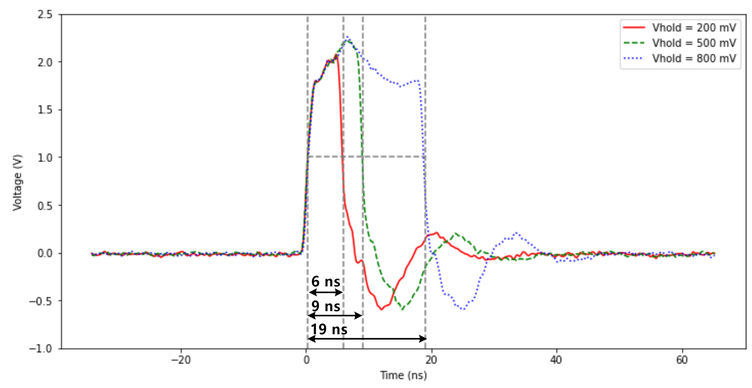


Fig. 9. Hold-off time measurements. (Red solid: 200 mV, Green dashed: 500 mV, Blue dotted: 800 mV applied at $V_{hold\text{-}off}$).

- Fig. 7 displays the simulation result of quenching performance. The conventional active quenching circuit takes about 4.55 ns to reach half VDD, while the proposed active quenching circuit takes about 1.59ns, almost three times faster.
- The measurement result of passive quenching is shown in Fig. 8. The DCC technique dramatically improved the rise time from 80 ns to 45 ns, proving its effectiveness.
- Fig. 9 shows the measurement result of hold-off time control. By controlling the bias voltage applied at $V_{hold\text{-}off,}$ desired hold-off time can be achieved.

## V. Conclusion

SPAD requires fast quenching to achieve a higher photon counting rate and minimize jitter and afterpulsing probability while maintaining compact active quenching size and affordable power consumption. In this work, the DCC technique boosting double active quenching of SPAD with minimized area overhead and low power has been designed in a 0.18 um CMOS technology. The simulation results confirm almost three times better quenching performance with an overhead of just a 23 % area increase compared to conventional design, while lowering power dissipation by 11 %. The proposed circuit also offers a programmable hold-off time of 5 ns to 50 ns. The measurement results show that boosted quenching results in 14 % lower jitter, making it suitable for ToF applications. It is also shown that the DCC technique effectively reduced the rise time of passive quenching down to 56 % compared to a simple passive quenching scheme.

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