Low Inductance Design for SNU X-pinch

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1. Introduction

An X-pinch is a sort of pinch effects using two or several crossed metal wires as a load [1]. Since a high-energy-density plasma (HEDP) and soft x rays are generated as a result, X-pinch experiments are widely used to research HEDP at laboratory level [2-4]. An X-pinch experiment requires sufficiently rapid and high current-rise rate (< 1 kA/ns), so total inductance of a X-pinch device should be low enough [4].

This research suggests new design of SNU X-pinch device to reduce total inductance. The effectiveness of these design in inductance reduction is evaluated through a 3D simulation and a simple circuit model.

2. Methods

2.1 Low inductance design

Fig. 1 shows cut-away view of the original device, excluding a vacuum chamber and capacitors, and two low inductance device designs. The modification has been made to the design of the capacitor bus-bars for reducing the volume surrounded by the bus-bars.

2.2 Simulation model

To calculate inductance of the X-pinch device, a short circuit test is simulated by CST Studio Suite®. Fig. 2 and 3 shows an example of a 3D simulation model and a circuit model used in this research.

The 3D simulation model includes only main current-carrying components of electrodes, a switch, capacitor bus-bars, and a short load. The short load is a cylinder with a diameter of 15 mm and a height of 10 mm. All conducting components are assigned as perfect electric conductor. Eight discrete ports are positioned where capacitors are installed. These ports are connected to ideal switches and 100 nF ideal capacitors in the circuit model. Another port is positioned between the electrode gap of the switch and connected to a probe for measuring total current and voltage. An external port is connected to each switch and closes them simultaneously.

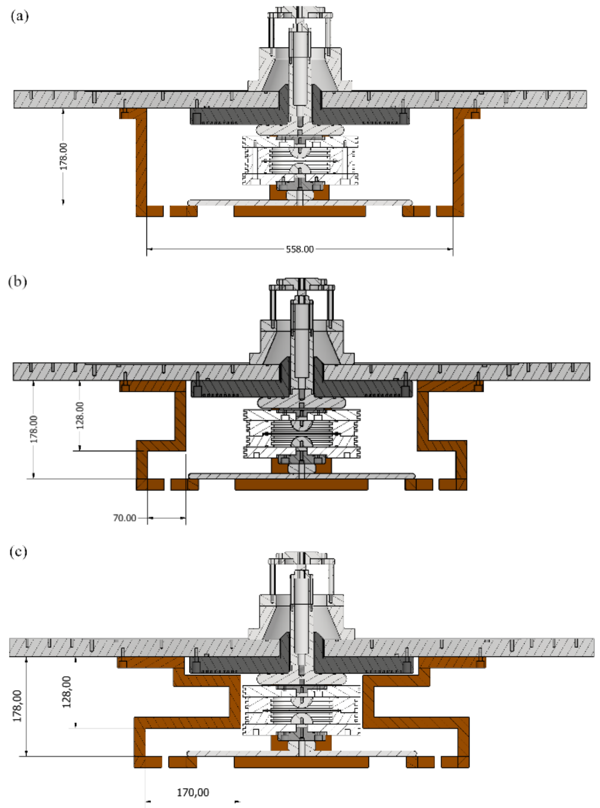

Fig. 1. Cut-away view of (a) the original SNU X-pinch device; (b), (c) low inductance device designs without a vacuum chamber and capacitors and low inductance device designs.

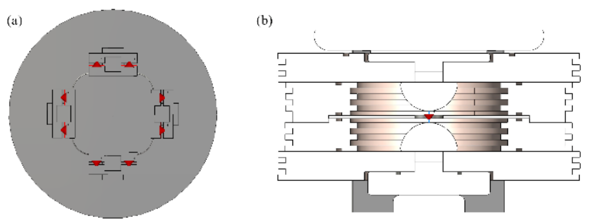

Fig. 2. An example of 3D simulation models. (a) Eight ports simulating capacitors, (b) a port to locate a probe. The ports marked in red.

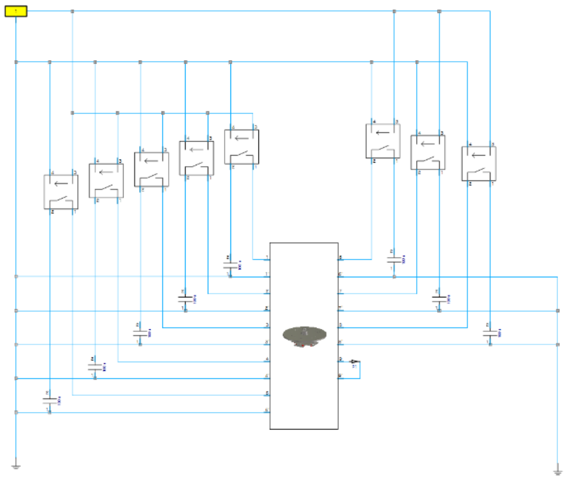

Fig. 3. An example of the circuit model. Each ideal capacitor has 100 nF capacitance and initially charged to 50 kV.

2.3 Experimental setup

A short circuit test is conducted to validate the simulation results. The capacitors are initially charged to 50 kV. The short load is a copper cylinder with the same dimensions as the load used in the simulation.

2.4 Inductance Calculation

Fig. 4 presents an example of simulation and experiment results. The equivalent circuit is analyzed as a series RLC circuit, and a damped sine curve is fitted to the result. The inductance of a chamber is extracted from the fitted curve using equation (1).

$$(1) \quad L = \frac{C}{\omega^2+\alpha^2}$$

where L is the total inductance, C is the total capacitance, ω is the angular frequency of the fitted curve, and α is the time constant of the fitted curve.

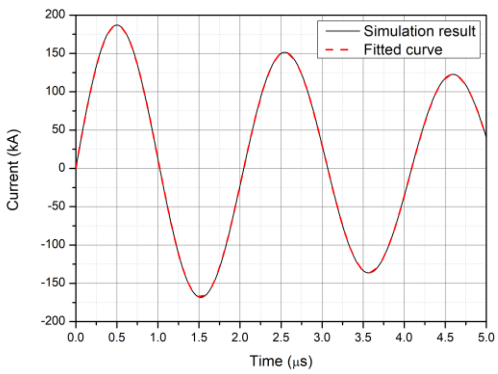

Fig. 4. An example of simulation results and fitted curves. A damped sine curve fits to the simulation result.

3. Results and Discussion

Table 1 presents the results of the experiment and simulations. The low inductance designs 1 and 2 correspond to the designs of Fig. 1-(b) and Fig. 1-(c) respectively. In the experiment, the measured total inductance is ~142 nH which is slightly larger than the simulation result of 135.93 nH. This is because parasitic inductance of capacitors and material of device is not considered. Nevertheless, the difference is sufficiently small to validate the simulation.

The total inductance of low inductance designs 1 and 2 estimated as 132.32 nH and 121.63 nH respectively. This indicates that the total inductance decreases when the volume surrounded by bus-bars is reduced. Therefore, it indicates that the suggested designs can reduce the total inductance of the device.

	Inductance (nH)
Experiment	~142
Original design	135.93
Low inductance design 1	132.32
Low inductance design 2	121.63

Table 1. Experiment and simulation results. Low inductance designs 1 and 2 correspond to the design of Fig. 1-(b) and Fig. 1-(c) respectively.

4. Conclusions

New designs to reduce total inductance of SNU X-pinch device is suggested. A 3D simulation model and a simple circuit model is used to calculate total inductance and validated through a short-circuit experiment. The suggested designs reduced total inductance of device effectively. These low inductance designs are useful to reduce the total inductance and achieve faster current-rise rate.

5. Acknowledgements

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