Performance Improvement of the LLRF Control System for the PEFP 100MeV Accelerator

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1. Introduction

The Proton Engineering Frontier project (PEFP) 20MeV proton linear accelerator has been operated for the RF and beam experiments in Korea Atomic Energy Research Institute (KAERI) site [1]. During the 20MeV accelerator operation, the stability of ±1% in RF amplitude and ±1° in RF phase is required at the Low-Level Radio Frequency (LLRF) control system. To meet these requirements, RF digital feedback control system has been developed and operated, which consists of a Field Programmable Gate Array (FPGA) control board and a LLRF analog system [2-3]. For the 100MeV accelerator operation, 11 LLRF control systems are required and it is necessary to improve performance of the LLRF control system. The upgrade and configuration of the LLRF control system to improve the RF feedback control is presented.

2. LLRF System Improvement

To improve the feedback control of RF amplitude and phase, Intermediate Frequency (IF) and Local Oscillator (LO) frequency to be used for the RF digital control is changed as summarized in Table 1. 10MHz IF and 40MHz sampling clock has been used for the RF field control of the 20MeV accelerator but 50MHz IF will be adopted for the 100MeV accelerator operation. They can be usually chosen with technological limitations including sampling rate and bit-resolution of the ADC and stability of the synthesized clock in the digital IQ detection scheme [4]. The choice of 50MHz IF reduces noise due to harmonic frequency components and spurious components so raise the stability of RF amplitude and phase in comparison to 10MHz IF.

Table 1: Frequency changes for the RF control

	20MeV accelerator	100MeV accelerator
RF	350 MHz	350 MHz
LO	340 MHz	300 MHz
IF	10 MHz	50MHz
Sampling clock	40 MHz	40 MHz

IQ modulation scheme is also changed to heterodyne up-conversion method to simplify the analog system with performance improvement of the LLRF control system. In the 20MeV operation, 2 DACs of the digital control board output I and Q signal and an analog IQ modulator has been used in the LLRF analog system [3]. The electric components to match signal condition between the DAC and the analog IQ modulator have been also used. In the heterodyne up-conversion scheme for the 100MeV accelerator operation, the digital control board outputs 50MHz IF signal and the IF signal is up-converted to 350MHz RF signal by mixing with 300MHz LO signal. This scheme doesn't need to use RF components of the IQ modulator and the matching circuit, so the LLRF analog system is simplified and noise is also reduced in the analog system.

3. LLRF System Configuration

The LLRF control system was configured to improve RF field control of the 100MeV accelerator. The commercial ICS-572B FPGA board, which has been operated for the digital feedback control in the 20MeV accelerator, was changed to the Pentek 7142 FPGA board. Figure 1 shows the Pentek 7142 FPGA board and the specifications are as follows.

- ADC : 125MHz max. sampling rate
  : 4 ch., 14bit resolution
- DAC : 320MHz max. converting rate
  : 1 ch., 16bit resolution
  : dc to 160MHz IF output
- FPGA : Xilinx Virtex4 XC4VSX55
- Memory : DDR2 SDRAM (64M×32)
- Clock : external (1 to 300MHz, 0 to +10dBm)
  : internal (125MHz max.)
- Gate : internal or external

Fig. 1: Pentek 7142 FPGA board

Fig. 2: LLRF analog system

The LLRF analog system was also manufactured as shown in Figure 2. This system performs up-down conversion, clock and reference signal distribution, and RF interlock for the HPRF protection. The linear power supply and RF seal was installed to reduce noise.

EPICS control system based on VME for the LLRF control system operation was built and Figure 3 shows the operator interface (OPI) based on EPICS IOC.

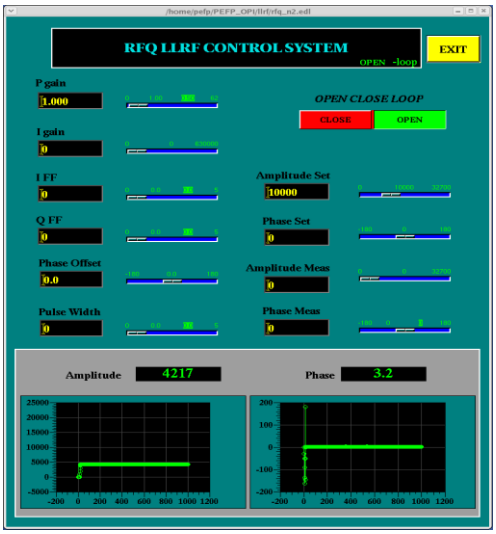

Fig. 3: Operator interface for the LLRF control system operation

4. LLRF System Test

LLRF control system has been tested by using the dummy cavity. Figure 4 shows RF waveforms measured in the LLRF test. 50MHz IF from the digital board and 350MHz RF was measured.

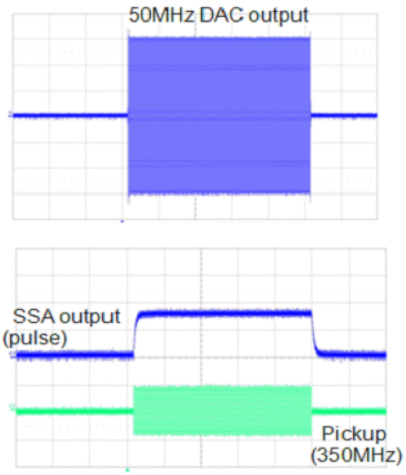

Fig. 4: RF waveforms measured in the LLRF test

5. Summary

Improvement of the LLRF control system was performed for the 100MeV accelerator operation. IF and LO frequency for RF feedback control was changed and IQ modulation scheme was also modified. LLRF control system for performance improvement was configured. The commercial FPGA control board was changed and the LLRF analog system was manufactured. The LLRF test has been tested by using the dummy cavity. This system will be operated for the PEFP 100MeV accelerator

Acknowledgements

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