Development of FPGA-Based Bistable Unit

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1. Introduction

It is well known that existing nuclear power plant (NPP) control systems contain many components which are becoming obsolete at an increasing rate. Various studies have been conducted to address control system hardware obsolescence [1]. Obsolete analog and digital control systems in non-nuclear power plants are commonly replaced with modern digital control systems, programmable logic controllers (PLC) and distributed control systems (DCS).

Field Programmable Gate Arrays (FPGAs) are highlighted as an alternative means for obsolete control systems. FPGAs are advanced digital integrated circuits (ICs) that contain configurable (programmable) blocks of logic along with configurable interconnects between these blocks. Designers can configure (program) such devices to perform a tremendous variety of tasks. FPGAs have been evolved from the technology of Programmable Logic Device (PLD). Nowadays they can contain millions of logic gates by nanotechnology and so be used to implement extremely large and complex functions that previously could be realized only using Application-Specific Integrated Circuits (ASICs) [2].

This paper is to present the development of a bistable unit which executes protection functions realized in FPGAs. Functional test is performed to verify its function. An Actel ProASIC3 FPGA platform is implemented as the bistable unit for Plant Protection System (PPS).

2. FPGA-Based Bistable Unit

In this section the configuration and operation of the FPGA-based bistable unit are described.

2.1 Basic Function

The PPS continuously monitors selected parameters to determine if a reactor trip or a safeguard initiation is required. The FPGA-based bistable unit receives measurements of selected parameters. There is one comparator function per parameter. The comparator compares the conditional digital value against a predetermined value to determine whether or not the sensed parameter has been exceeded. Finally, the bistable unit transmits the results of comparison to the Local Coincidence Logic (LCL) units and system monitoring data to Maintenance and Test Panel (MTP).

2.2 Physical Description

The bistable unit is fully modular with modules mounted in 19-inch chassis. Refer to Figure 1. The bistable unit consists of DC power supplies, a digital input module, comparator modules, and communication interface modules. It also contains a backplane that provides for distribution of power and for data signal transmission among the modules. Each module has not any Central Processing Unit (CPU) and Operating System (OS).

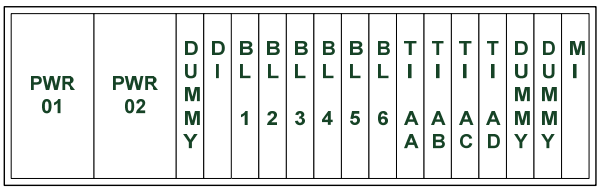

Fig. 1. Configuration of FPGA-based bistable unit

The digital input module accepts up to 32 digital inputs (24 Vdc) per module and includes input optical isolation, contact bounce filtering and front module input status indicators.

Each comparator module has analog input channels, digital input channels and Actel ProASIC3 FPGAs and other necessary circuit elements. It accepts up to 4 analog differential inputs per module, with 16-bit resolution, and up to 4 contact status inputs.

Communication interface modules provide RS-422 serial ports with the maximum data rates of 19,200 bit/s for data transmission.

2.3 System Operation

2.3.1 System Inputs

The FPGA-based bistable unit receives the following types of input parameters sensed by the PPS.

- Analog inputs are 0-10 Vdc signals that vary directly as a function of the measured NSSS parameter. These input signals are converted to digital values via the comparator modules.

- Digital inputs are transmitted by the Core Protection Calculators (CPC), the Excore Neutron Flux Monitoring System (ENFMS) and PPS control panels. Digital input signals are sensed as contact inputs by the digital input or comparator modules. These inputs

are used for trip parameter, operating bypass, setpoint reset, etc.

- Communication inputs are serial data from the MTP for bistable bypass and setpoint reset.

2.3.2 Bistable Processing

The FPGA-based bistable unit receives operation commands from the ENFMS and PPS control panels, such as operating bypass, bypass permissive, setpoint reset, etc. The digital input module receives command signals and transmits them to the comparator modules via backplane.

The comparator modules directly receive analog inputs and some of digital inputs which are trip parameters of the PPS such as pressures, level, flows, local power density, etc. The signals are compared against predetermined or calculated limits. The limits represent boundary condition, which should not be violated if the plant is to operate safely. The limits might also represent a condition in which some action is required to mitigate the consequences of a rupture in a pressure boundary. When a limit is violated the comparator module generates a trip output for that parameter. The trip output is passed to one LCL unit in the channel and to one LCL unit in each of the other three channels via trip interface modules.

Figure 2 presents the typical block diagram of comparator logic incorporated into a FPGA [3]. The FPGA is programmed with Very-High-Speed Integrated Circuits (VHSIC) Hardware Description Language (HDL). FPGA hardware description is to describe electrical signal flows among logic gates in the FPGA. The hardware description of the FPGA-based control board is developed using the Libero integrated design environment (IDE) which is Actel's comprehensive software toolset for designing with all Actel FPGAs [4].

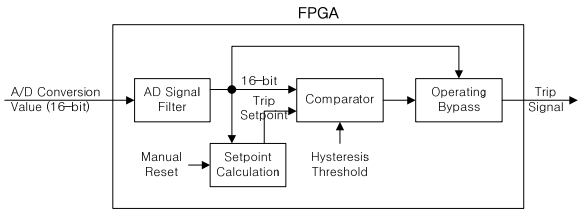

Fig. 2. Comparator logic incorporated into FPGA

The process inputs are listed in Table 1. This table correlates the process input assignments with the comparator modules. The table also correlates the process inputs with their associated bistable functions.

The FPGA-based bistable unit communicates with the MTP via a monitoring interface module. It receives operation commands from the MTP and provides status information to the MTP.

Table 1. Input Parameters and Trip Function Characteristics

Input Parameter	Allocated Module	Bistable Type	Setpoint Type
Linear Power	BL 5	Rising	Rate Variable
Log Power	BL 4	Rising	Fixed
PZR Pressure NR	BL 5	Rising	Fixed
PZR Pressure WR	BL 6	Falling	Reset Variable
SG1 Level WR	BL 3	Falling	Fixed
SG2 Level WR	BL 4	Falling	Fixed
SG1 Level NR	BL 1	Rising	Fixed
SG2 Level NR	BL 2	Rising	Fixed
SG1 Pressure	BL 3	Falling	Reset Variable
SG2 Pressure	BL 4	Falling	Reset Variable
SG1 RCS Flow	BL 1	Falling	Rate Variable
SG2 RCS Flow	BL 2	Falling	Rate Variable
Containment Pressure NR	BL 3	Rising	Fixed
Containment Pressure WR	BL 6	Rising	Fixed
Refueling Water Level	BL 4	Falling	Fixed
Local Power Density	BL 3	Contact	-
DNBR	BL 4	Contact	-

3. Conclusions

This paper is to address function, configurations and operation related to a FPGA-based bistable unit developed by Korea Power Engineering Company (KOPEC).

It has been demonstrated that all bistable logic algorithms of the PPS can be realized with the FPGA-based bistable unit. The developed bistable unit, without any CPU and OS, accurately generates bistable trip signals when a trip parameter exceeds its setpoint. The bistable unit provides separate circuits per trip parameter and parallel processing of all parameters from signal inputs to comparator outputs due to the characteristics of FPGAs and module design.

In conclusion, FPGAs make it possible to develop a simple hardware platform easy to understand. It is expected that FPGAs are going to improve the safety and availability of the plants.

REFERENCES

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[3] Yoon Hee Lee, See Chae Jeong, Woong Seock Choi, Chang Jae Lee, Jin Kwon Jeong, and Jae Hong Ha, "Development of FPGA-Based Control Board", Transactions of the Korean Nuclear Society Autumn Meeting, 2009.
[4] Actel Corporation, "Actel Libero IDE User's Guide", v8.6.