Development of FPGA-Based Control Board

Yoon Hee Lee *, See Chae Jeong, Woong Seock Choi, Chang Jae Lee, Jin Kwon Jeong, Jae Hong Ha
Korea Power Engineering Company Inc., 150 Yuseong-Gu, Deokjin-Dong, Daejeon, Korea, 305-353
**Corresponding author: yhlee4@kopec.co.kr*

1. Introduction

It is well known that existing nuclear power plant (NPP) control systems contain many components which are becoming obsolete at an increasing rate. Various studies have been conducted to address control system hardware obsolescence [1]. Obsolete analog and digital control systems in non-nuclear power plants are commonly replaced with modern digital control systems, programmable logic controllers (PLC) and distributed control systems (DCS).

Field Programmable Gate Arrays (FPGAs) are highlighted as an alternative means for obsolete control systems. FPGAs are advanced digital integrated circuits (ICs) that contain configurable (programmable) blocks of logic along with configurable interconnects between these blocks. Designers can configure (program) such devices to perform a tremendous variety of tasks. FPGAs have been evolved from the technology of Programmable Logic Device (PLD). Nowadays they can contain millions of logic gates by nanotechnology and so be used to implement extremely large and complex functions that previously could be realized only using Application-Specific Integrated Circuits (ASICs) [2].

This paper is to present the development of a FPGA-based control board performing user-defined control functions. An Actel ProASIC^{plus} FPGA platform is implemented as the comparator of Plant Protection System (PPS). Functional simulation is implemented for the comparator.

2. FPGA-Based Control Board

The FPGA-based control board outlined in Figure 1 has two (2) analog inputs, two (2) analog outputs, twelve (12) digital inputs, twelve (12) digital outputs, one (1) Actel ProASIC^{plus} FPGA and other necessary circuit elements.

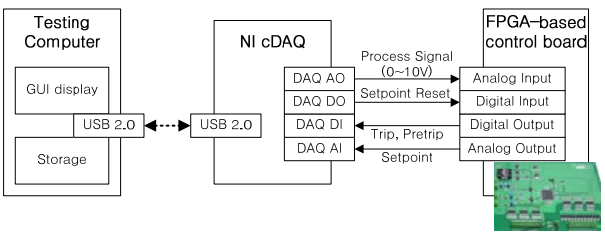

Fig. 1. FPGA-based control board and functional simulation environment

0-10V analog signals are inputs to an A/D converter with 16-bit resolution. The 16-bit binary digital signals are inputs to the FPGA system. Also, 16-bit binary digital signals are outputs from the FPGA system. 0-10V analog signals are outputs from a D/A converter with 16-bit resolution. 24V discrete signals are direct input to and output from the FPGA.

The Actel ProASIC^{plus} FPGA [3] is a collection of abundant logic tiles and routings. Each logic tile can be configured into 3-input/1-output logic function by programming the appropriate flash switches. The configurability of both logic tiles and routings provides great flexibility in realizing digital control systems. The ProASIC^{plus} FPGAs are manufactured with flash-based technology. Because they are nonvolatile, they always retain their configuration and so are “instant on” when power is first applied to the system. ProASIC^{plus} also provides reprogrammability, firm error immunity, and enhanced security to protect sensitive Intellectual Property (IP).

The FPGA-based control board realizes variable overpower trip logic and low pressurizer pressure trip logic. Simplified trip logic, presented in Figure 2 is incorporated into the ProASIC^{plus} FPGA.

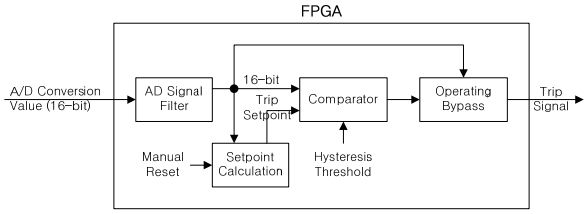

Fig. 2. Trip logic incorporated into FPGA

The FPGA is programmed with Very-High-Speed Integrated Circuits (VHSIC) Hardware Description Language (HDL). FPGA hardware description is to describe electrical signal flows among logic gates in the FPGA. The hardware description of the FPGA-based control board is developed using the Libero integrated design environment (IDE) which is Actel’s comprehensive software toolset for designing with all Actel FPGAs [4].

The variable overpower trip logic generates trip signals when the indicated neutron flux power increases at a great enough rate or reaches a high preset value. This trip function uses a rate-limited variable setpoint presented in Figure 3. A hysteresis threshold is provided to prevent jitter in the trip signal.

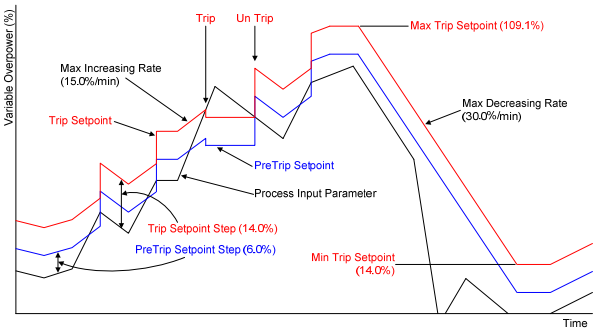

Fig. 3. Rising trip variable setpoint with automatic rate limiting

The low pressurizer pressure trip logic generates trip signals when the measured pressurizer pressure falls to a low predetermined value shown on Figure 4. The trip logic includes an operating bypass. This operating bypass is manually enabled below a predetermined pressure and automatically removed above a preset pressure. A hysteresis threshold is provided to prevent jitter in the trip signal.

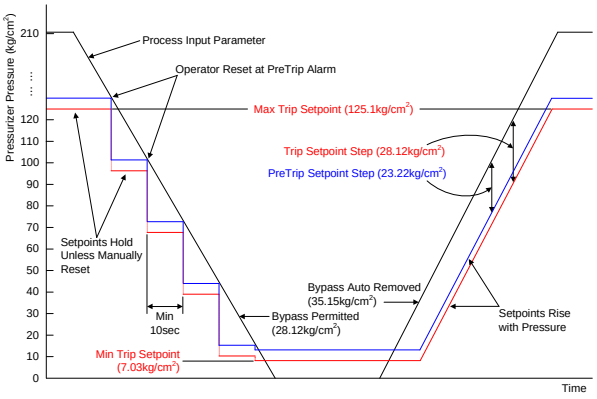

Fig. 4. Falling trip variable setpoint with manual reset

3. Functional Simulation Environments

The functional simulation platform outlined in Figure 1 is composed of three major components; a testing computer providing man-machine interfaces, National Instruments (NI) DAQ interface and the FPGA-based control board.

National Instrument (NI) cDAQ-9172 series are utilized to provide electrical connection between the external control cards and simulation computer. The simulation computer requires the cDAQ-9172 to generate process input signals in Figure 3 and 4. The process input signals requested via a USB port are then converted to analog (0-10V) values through NI analog output cards and sent to the external control board. Monitored variables are simply stored in a computer hard disk and displayed on a computer monitor as shown on Figure 5.

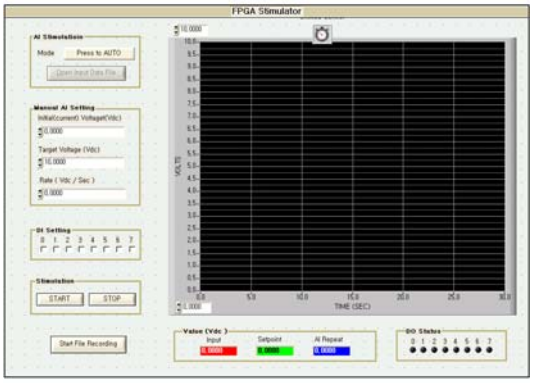

Fig. 5. GUI display

The GUI display provides the following set-ups:

1. Starting or stopping the stimulator
2. Generating virtual process signals manually or automatically
3. Monitoring and/or saving input/output signals

3. Conclusions

This paper is to address configurations and functional simulation environments related to a FPGA-based control board. The control board realizes the most complicated bistable logic of the PPS: variable overpower trip logic and low pressurizer pressure trip logic.

In conclusion, the FPGA-based control board accurately provides bistable trip signals when a trip parameter exceeds its setpoint in Figures 3 or 4. The time delay of the digital device today is shorter and shorter with the development of CMOS technology. Nanosecond level is not a goal that could not be reached any more, thus the PPS response time can be shortened by using the advanced FPGA [5]. It is expected that FPGAs are going to improve the safety and availability of the plants.

REFERENCES

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