Performance Evaluation of a Network the Switch for SMART Safety I&C Systems

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1. Introduction

Process or control signals of safety-grade I&C systems in an NPP(Nuclear Power Plant) are generated periodically. These signals should be delivered to each destination within the predefined response time limit over the safety network. Therefore, communication networks in NPPs should be deterministic. The network switch of a star topology has to be designed to meet the required response time and deterministic characteristics.

In this paper, we introduce performance evaluation and design considerations for a safety network switch which is under development.

2. Network Switch

The network switch of this paper should have a deterministic behavior for industrial or nuclear application where process data or control data has to be delivered within a certain time limit.

Recently, the performance of switched Ethernet shows deterministic characteristics by elimination of uncertainties in the network switch structure and operation [1].

We proposed the design concepts of a network switch which have a star topology, separation between an input and output line interface, an optic fiber, a shared bus and a full duplex operation with two simplex physical links [2]. Figure 1 shows the structure of a network switch.

2.1. The operation of a network switch

In this section, we present the design concept and architecture of the network switch which is specially designed to meet all requirements of applications in NPPs.

Architecture of the network switch for an NPP is shown in Figure 1. The network switch has tens of line interfaces to connect other nodes. Each line interface has two independent buffers: a TX buffer, and an RX buffer which are physically separated.

A store & forward method is used for packet delivery in the network switch. When a line interface receives a packet, the processor of the network switch inspects the destination address in the header of a packet and forwards it to the designated interface. In other words, a packet is stored in the TX buffer of the designated line interface and the line interface controller transmit packets which are stored in the TX buffer on a first-come-first-served(FCFS) basis.

The line interface in network switch operates in full duplex mode. Communication media for the transmitter and receiver are physically independent. Therefore, there is no collision or contentions while data processing.

Since packet process speed is fast enough to accommodate all line interface capacities, many connected nodes can communicate without collision and contention while keeping delay time under a certain value.

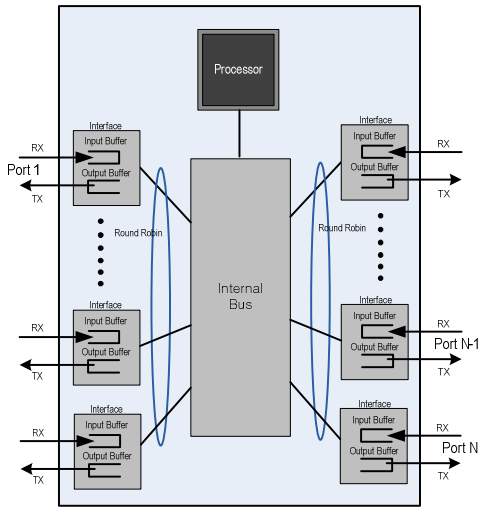

Figure 1. The structure of a network switch

2.2. Performance requirement

The network switch should satisfy the following requirements to meet deterministic characteristics in NPP applications.

1) The number of packet processing per unit time in the network switch should be more than the number of packets generated in all nodes per unit time
2) The capacity of a line interface should be larger than the traffic ingress to line interface.

If a lot of packets forwarded to the specific line interface simultaneously, traffic may excess the transmission capacity of the line interface. One or more packets could be waiting to transmit in the TX buffer and it increases the queuing and end-to-end delays. Also, the small size of the buffer could cause a packet loss by buffer overflow. To solve this problem, we need to analyze the traffic pattern and derive an appropriate performance requirement from it. Another solution is that traffic is properly managed.

The network switch we describe here has 32 line interfaces whose capacity is 10-Mbps with optical fiber for physical media. Each port of the line interface serves as in a round-robin manner, and switching fabric is a shared bus.

2.2 .1. Packet-processing performance

We address the required packet processing performance to meet requirements mentioned in section 2.2. PPS (Packets Per Seconds) is one of the major performance metrics in commercial communication devices. It indicates how many packets a switch can handle per second. The size of packet typically sets to 64 bytes.

Because our switch has 32 line interfaces and each line interface has a 10-Mbps capacity, we can calculate the minimum PPS as follows:

Number of ports × Capacity per port/size of packet
= 32×10,000,000/(64×8) = 625,000 pps

It means that our switch should be able to process at least 625,000 packets per second. The required time to process one packet is less than 1.6 usec.

32 line interfaces are served by round robin manner ,as shown in Figure 1. The maximum time requirement to complete one round (from first to 32rd line interface) is ;

1.6usec. × 32(port) = 0.0512msec.

2.2 .2. Buffer size of line interface

The network switch should prevent packet loss from buffer overflow. It can be caused by excessive traffic over the line interface capacity or burst traffic in a short time.

Let us consider the worst case scenarios of traffic pattern, as follow:

- Packets of N-1 ports move toward the same port at the same time.
- The average traffic ingress to one port should not exceed the capacity of the port, 10-Mbps

The required buffer size is more than the packet size times the number of ports in order to avoid packet loss by buffer overflow. Excessive traffic for a short time is called “burst traffic” which causes inevitably long delay.

2.2 .3. Transmission delay

End-to-end response time is an important factor for the overall MMIS system in an NPP.

As the transmission delay inside the network switch has a large end-to-end response time, Transmission delay analysis is required.

The transmission delay of the network switch is expressed in the following simple formula;

$$T_{total} = T_{rx} + T_{rr} + T_{pr} + T_{tx}$$

where T_{total} is the overall transmission delay in the switch, T_{rx} is the packet reception time in the Rx port, T_{pr} is the processing time, T_{rr} is the waiting time to be served by a processor and T_{tx} is the packet transmission time in Tx port.

For the estimation of T_{total} , we assume that all nodes send a 64-bytes message in every certain time (e.g., 25msec.).

Table 1. Transmission delay inside the network switch

	Min. value	Max. value
Transmission delay in the switch	0.104 msec	0.1536 msec.

The time for processing a single 64-bytes-sized packet is in the range of 0.104ms and 0.1536m (Table 1). Therefore, we can say that our switch has deterministic characteristics because it has predictable latency.

2.3. Performance consideration

The network switch has several functions in addition to its own duty such as traffic monitoring and reporting its current status. Numerical values addressed in the previous section do not consider the process overhead for other tasks. Hardware performance of the network switch is faster than the addressed numerical value by at least 50%.

3. Conclusions

In this paper, the network switch which has a star topology and full duplex operation using two simplex transmissions is presented. The performance evaluation of this network switch is performed. To satisfy the deterministic characteristics and the system response time, the packet-forward operation of the network switch should be cyclically performed with each line interface(for example, by round-robin method or polling), and the buffer size of each line interface should be sufficient to avoid packet loss.

Based on the performance evaluation, the implementation process is underway. Future studies should examine the performance measurement of the network switch hardware prototype based on this work.

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