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Arc Energy Limiting Mechanism of the High Voltage Converter Modulator

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1. Introduction

A 100MeV proton accelerator is being developed at Proton Engineering Frontier Project (PEFP). The RF duty of the 20MeV~100MeV DTL is 9% whereas that of 20MeV DTL is 24%. Therefore it is advantage to use a pulse modulator for 9% duty machine. A high voltage converter modulator (HVCM) will be used as a pulse modulator for 100MeV DTL klystron. The power rating of the HVCM is such that it can drive two klystrons simultaneously whereas one klystron drives one DTL tank. The schematics of the RF system for the 100MeV DTL is shown in Fig. 1. One of the advantages of the HVCM is its self protecting mechanism against the load arc. In other words, it needs not a load arc limiting device to protect the klystron from arc energy. In this paper, the self protecting mechanism of the HVCM is discussed through circuit analysis and test plan is presented.

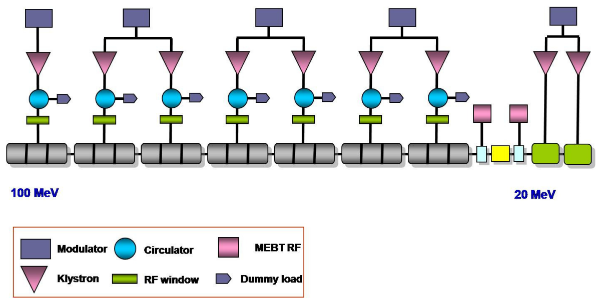

Fig. 1: Layout of the RF system for 100MeV DTL

2. High Voltage Converter Modulator

There are several options for the long pulse (>1ms), high average power klystron power supply. Those are the hard tube type pulse modulator used at LANSCE and J-Parc, bounce circuit used at TTF [1], HVCM used at SNS [2]. The advantages of the HVCM are its small volume, its voltage regulation capability at flat top, and self protecting mechanism against load arc. As shown in Fig. 1. 5 sets of HVCM will be used for the 100MeV proton accelerator. The specification of the HVCM for 20~100MeV proton accelerator is as follows.

- Input voltage : 3300Vac
- Input frequency : 60Hz
- Output DC voltage : -105kV, +10%, -50%
- Output current : 50ADC
- Output peak power : 5.8MW
- Output average power : 520kW at 9% duty
- Efficiency > 92%
- HVCM waveform : square wave
- Pulse width : 1.5ms
- Max. repetition rate : 60Hz
- Flat top regulation : 1%
- Flat top voltage droop : 1%
- Pulse rise time : < 0.1ms
- Pulse fall time : < 0.1ms
- Flat top minimum : 0.1ms
- Arc energy : <20J

The circuit diagram of the HVCM is shown in Fig. 2. The first HVCM has been delivered to the KAERI site, the second one will be tested at October, 2009. The third one is being processed for purchase order.

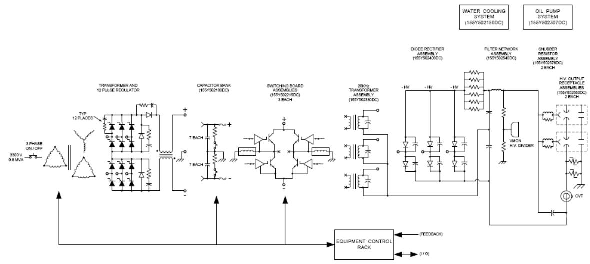

Fig. 2: HVCM circuit diagram

3. HVCM Circuit Analysis

The simplified circuit diagram seen from the 2nd side of the high voltage transformer is shown in Fig. 3. The source was considered as a voltage source with 94% fixed duty. The switching frequency was 20kHz. The leakage inductance of the transformer (La, Lb, Lc) and shunt peaking capacitor (Ca, Cb, Cc) constitute a resonant circuit.

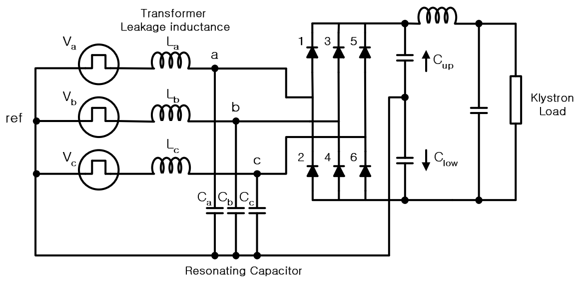

Fig. 3: Simplified circuit diagram seen from second side of the high voltage transformer

The load voltage and current profile were analyzed and the results are shown in Fig. 4 and Fig. 5. As shown in the Fig. 5, the operation mode can be divided into three regions in single current conduction period through a diode (designated with rectangle). The capacitor supplies current into the inductor in resonant condition as designated with triangle. A variable resistor is connected in parallel to the load resistance to simulate the load arc case. The variable resistor has infinite resistance value at first and has low resistance value such as 1ohm after 0.5ms. The load voltage and current profile using this circuit is shown in Fig. 6. The voltage decreases abruptly and the current increases at arc condition. The current through the resonating capacitor decreases to zero in the load arc condition which means the resonant condition is detuned as shown in Fig. 7. The load current and inductor current increase in the analysis. But the transformer reaches saturation and the IGBT opens with over current condition, when there is a load arc in real situation, which drive the self protecting mechanism of the HVCM.

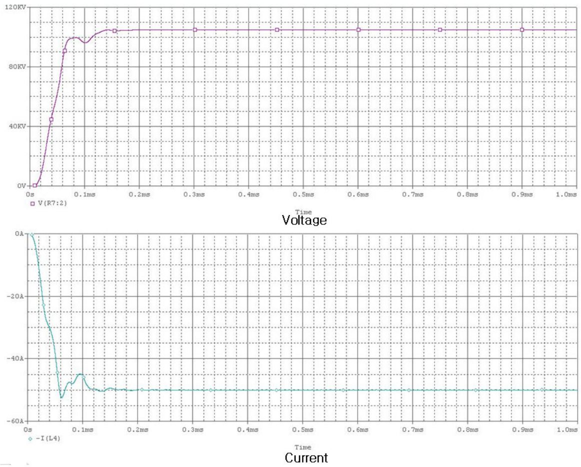

Fig. 4: Load voltage and current profile during normal operation

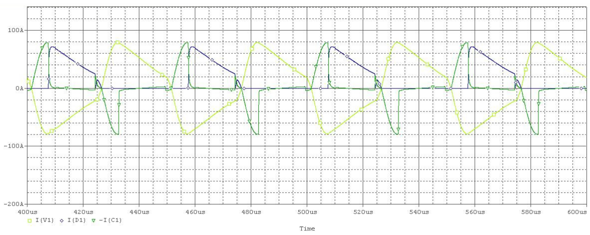

Fig. 5: Current in the leakage inductance, resonant capacitor and diode during normal operation

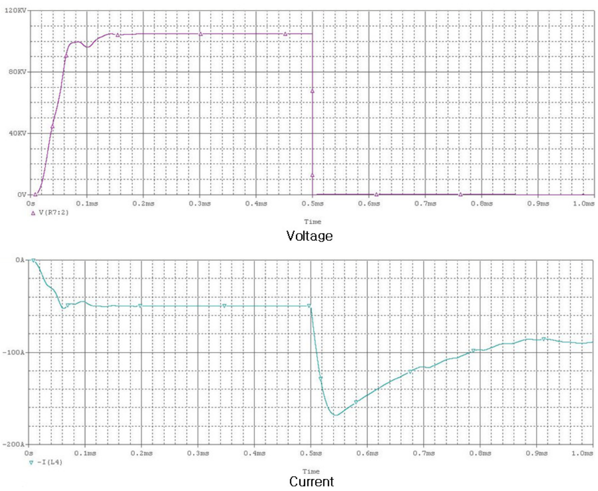

Fig. 6: Load voltage and current profile during arc condition at 0.5ms

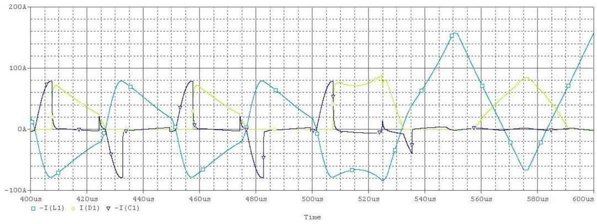

Fig. 7: Current in the leakage inductance, resonant capacitor and diode during arc condition

4. Test Plan

The first HVCM has been delivered in the KAERI site as shown in Fig. 8. The system consists of control system rack, SCR unit, high voltage converter modulator which includes oil tank basket, capacitor bank, IGBT switching plates, and tank assembly. The system will be assembled, installed and tested with 2.1kohm, 20kW dummy load at low duty. After the test with the dummy load, the HVCM will be connected to the two klystrons to drive the 20MeV accelerator RF system which is already installed at KAERI site.

Fig. 8: Tank assembly and capacitor bank

Acknowledgement

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[2] D. E. Anderson, J. Hicks, M. Wezensky, D. Baca, W. Reass, Operational Performance of the Spallation Neutron Source High Voltage Converter Modulator and System